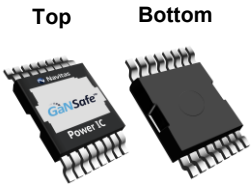
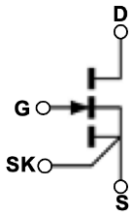
GaN-FET



Top-cooled
TOLT-16L



Simplified Diagram

1. Features

- V_{DS} 650V continuous / 800V transient
- 25 mΩ $R_{DS(ON)_MAX_25C}$ and 90 A $I_{DS(CONTINUOUS)}$
- TOLT-16L thermally-enhanced, top-cooled
- Zero reverse-recovery charge
- RoHS, Pb-free, REACH-compliant

2. Applications / Topologies

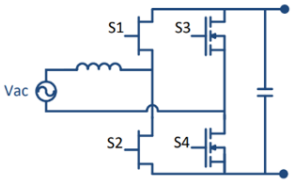
- AC-DC, DC-DC, CCM or CRM TP-PFC
- Optimized for synchronous half-bridge, full-bridge, 3-phase, or buck/boost operation
- Data Center CRPS, and Solar Inverter/ESS
- EV OBC & DC-DC converter, and motor GS

3. Description

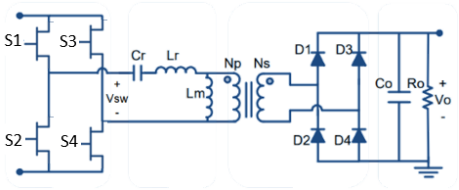
The NV6064 is a thermally-enhanced top-cooled SMD version of the Discrete GaN, optimized for higher power systems using GaNFET™ technology, making it the ideal choice for high-frequency, high-power-density, and high-efficiency power systems in data center, solar, industrial, and automotive segments.

The TOLT package ties this architecture together with industry-standard thermally-enhanced packaging, creating dependable solutions for world-class size/weight, efficiency, and cost.

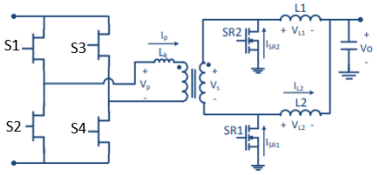
4. Typical Application Circuits



BTP PFC



CLLC or LLC



PSFB or DAB

5. Absolute Maximum Ratings (Note 1) (with respect to Source, T_{CASE} = 25°C, unless specified)

Symbol	Parameter	Max	Units
$V_{DS(CONT)}$	Continuous Drain-to-Source voltage	-7 to +650	V
$V_{DS(TRAN)}$	Transient Drain-to-Source voltage (Note 2)	800	V
$I_{DS(CONT)}$	Continuous Drain current (T_{CASE} = 25 °C) (Note 3) Continuous Drain current (T_{CASE} = 100 °C, T_{JUNC} = 150 °C) (Note 3)	90 57	A
I_{DS_PULSE}	Pulsed Drain current (10 µs @ T_{JUNC} = 25 °C) (Note 3) Pulsed Drain current (10 µs @ T_{JUNC} = 150 °C) (Note 3)	175 80	A
V_{GS}	Continuous input voltage measured between V_G and SK pins	-10 to 7	V
$V_{GS\text{-}TRANS}$	Transient input voltage measured between V_G and SK pins (Note 4)	-2.0	V
dV/dt	Slew Rate on Drain-to-Source	100	V/ns
T_{JUNC}	Junction Temperature	-40 to +150	°C
T_{STOR}	Storage Temperature	-55 to +150	°C

(1) Absolute Maximum Ratings are stress ratings, and subjecting devices to stresses beyond these ratings may cause permanent damage.

(2) $V_{DS(TRAN)}$ allows for surge ratings during ***non-repetitive*** events that are < 100 µs.

(3) Limited by Saturation.

(4) Limited to 200 ns.

6. Recommended Operating Conditions (Note 5)

Symbol	Parameter	Min	Typ	Max	Units
V_{GS_H}	GS input pin voltage high		6.5		V

(5) Exposure to conditions beyond maximum recommended operating conditions for extended periods of time may affect device reliability.

7. Thermal Resistance

Symbol	Parameter	Typ	Units
$R_{\theta_JUNC-CASE}$	Junction-to-Case Thermal Resistance	0.28	°C/W

8. Electrical Characteristics

Conditions unless otherwise specified: V_{DS} = 400V, V_{GS} = 6V, T_{CASE} = 25°C, I_{DS} = 29A, R_G = 5Ω

Symbol	Parameter	Min	Typ	Max	Units	Conditions
GaN FET Characteristics						
I_{DSS}	Drain-Source leakage current		4.5	100	μA	V_{DS} = 650 V, V_{GS} = 0 V
I_{DSS}	Drain-Source leakage current		45		μA	V_{DS} = 650 V, V_{GS} = 0 V, T_{JUNC} = 150 °C
I_{GSS}	Gate-Source leakage current		255		μA	V_{GS} = 6.5V
$R_{DS(ON)}$	Drain-Source resistance		18	25	mΩ	V_{GS} = 6V, I_{DS} = 29 A
$R_{DS(ON)}$	Drain-Source resistance		43		mΩ	V_{GS} = 6V, I_{DS} = 29 A, T_{JUNC} = 150 °C
V_{SD}	Source-Drain reverse voltage		3.3		V	V_{GS} = 0 V, I_{SD} = 29 A
I_{SD}	Source-Drain reverse current		150		A	V_{GS} = 0V, V_{SD} = 7V, 50us pulse, based on $P_{DISSIPATION}$
C_{OSS}	Output capacitance		143		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{ISS}	Input capacitance		620		pF	V_{DS} = 400 V, V_{GS} = 0 V
C_{RSS}	Reverse Transfer capacitance		0.9		pF	V_{DS} = 400 V, V_{GS} = 0 V
Q_{OSS}	Output charge		125		nC	V_{DS} = 400 V, V_{GS} = 0 V
Q_{RR}	Reverse recovery charge		Zero		nC	
Q_{GATE}	Total Gate charge		16		nC	V_{DS} = 400V, V_{GS} = 0V to 6.5V
Q_{GS}	Gate-to-Source charge		2.8		nC	V_{DS} = 400V, V_{GS} = 0V to 6.5V
Q_{GD}	Gate-to-Drain charge		4		nC	V_{DS} = 400V, V_{GS} = 6.5V
$C_{O(er)}$ (Note 6)	Effective output capacitance, energy related		206		pF	V_{DS} = 400 V, V_{GS} = 0 V
$C_{O(tr)}$ (Note 7)	Effective output capacitance, time related		314		pF	V_{DS} = 400 V, V_{GS} = 0 V

(6) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as C_{OSS} while V_{DS} is rising from 0 to 400 V

(7) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as C_{OSS} while V_{DS} is rising from 0 to 400 V

9. Inductive Switching Test Circuit and Typical Waveforms

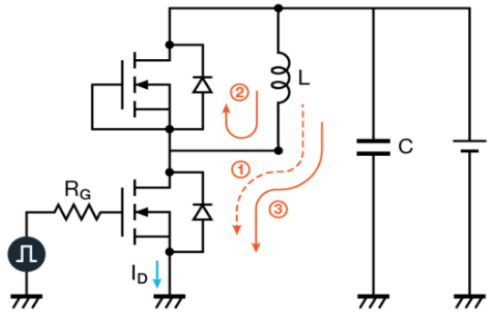


Fig. 1. Inductive Switching Test Circuit

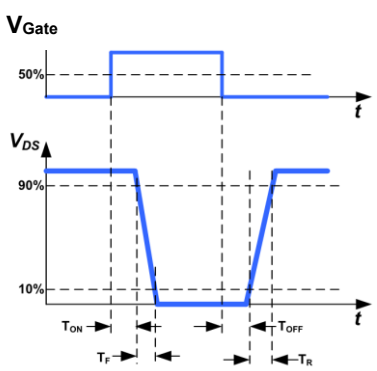


Fig. 2. Prop Delay, Rise/Fall Time

10. Electrical Curves (GaN FET, T_{CASE} = 25 °C unless otherwise specified)

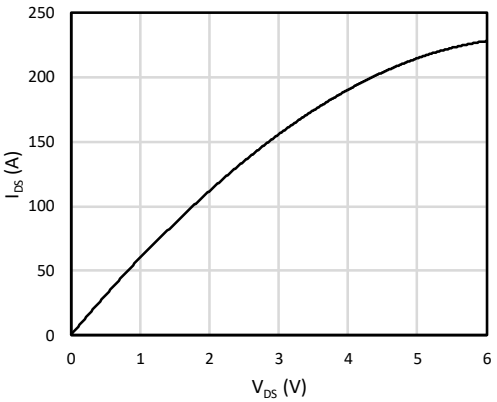


Fig. 3. I_{DS} vs. V_{DS}, V_{GS}= 6.5V, T_J = 25 °C

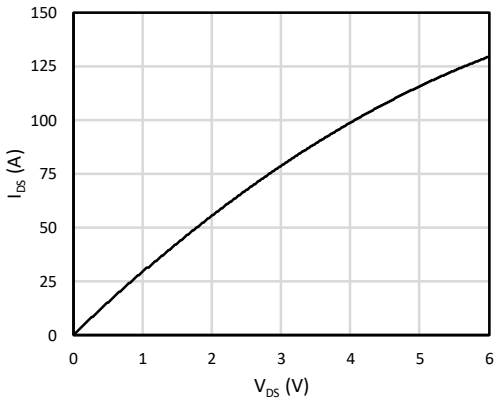


Fig. 4. I_{DS} vs. V_{DS}, V_{GS}= 6.5V, T_J = 150 °C

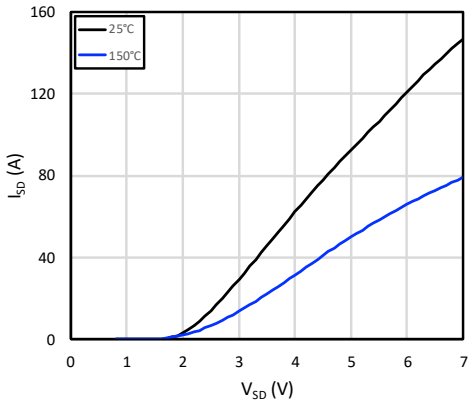


Fig. 5. I_{SD} vs. V_{SD}, V_{GS}= 0 V

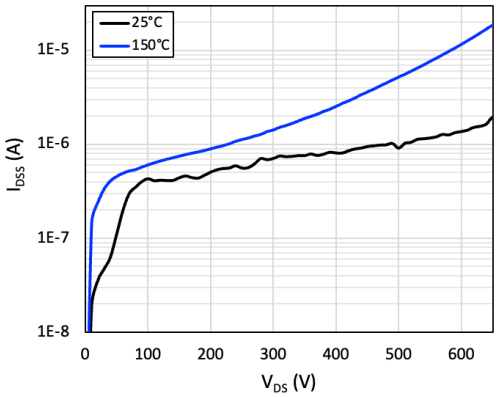


Fig. 6. I_{DSS} vs. V_{DS}, V_{GS}= 0 V

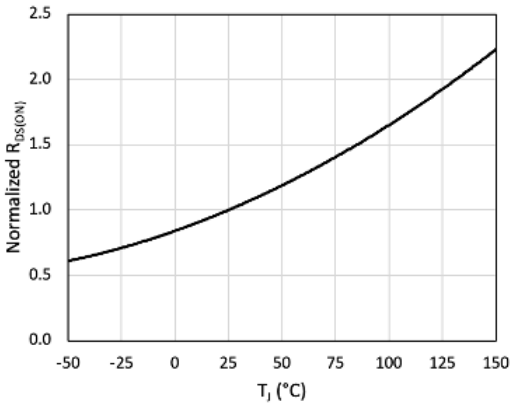


Fig. 7. Normalized R_{DSON} vs. T_{JUNC}

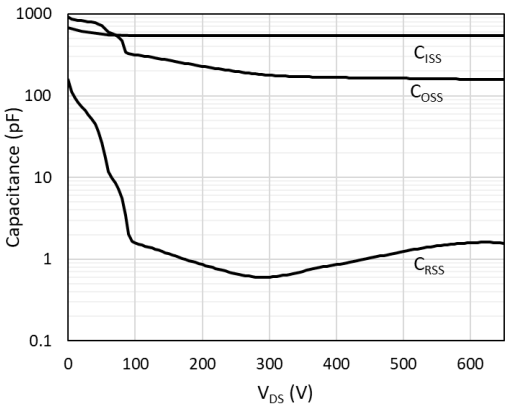


Fig. 8. C_{ISS}, C_{OSS}, C_{RSS} vs. V_{DS}

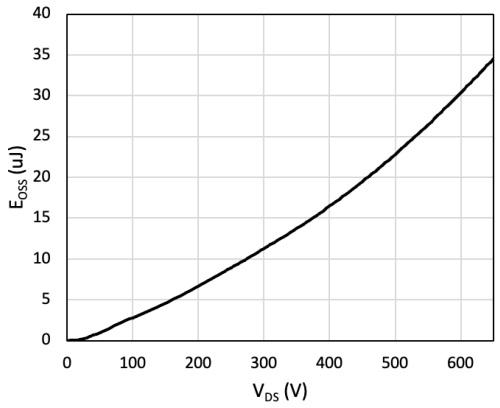


Fig. 9. E_{OSS} vs. V_{DS}

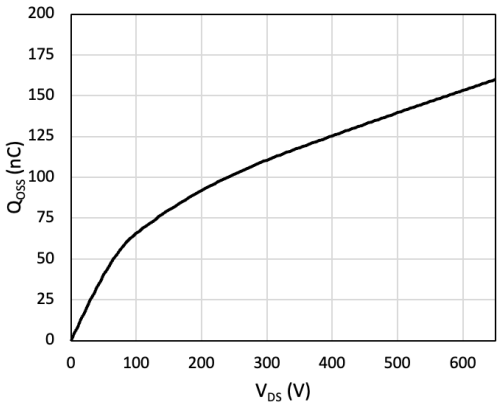


Fig. 10. Q_{OSS} vs. V_{DS}

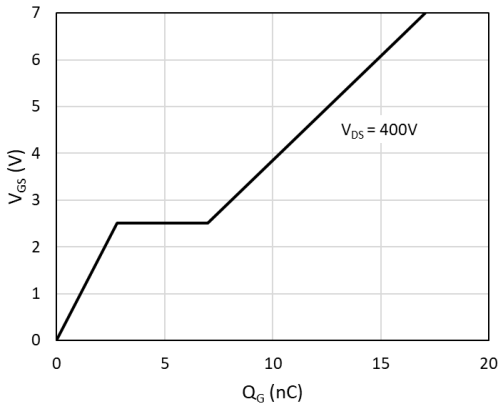


Fig. 11. V_{GS} vs. Q_{GATE}

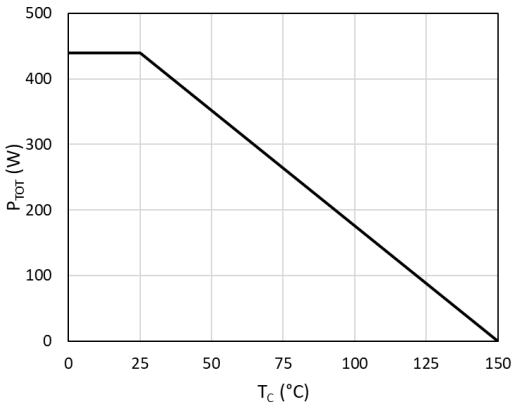


Fig. 12. $P_{DISSIPATION}$ vs. T_{CASE}

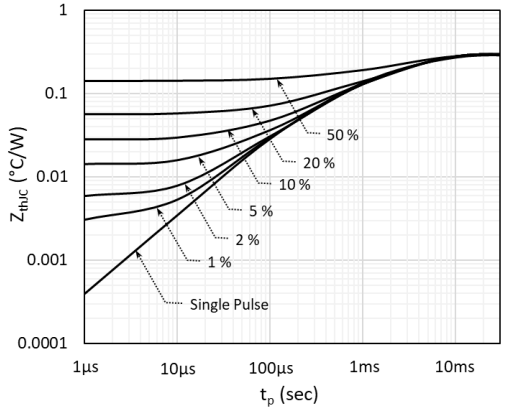


Fig. 13. Transient $R_{\Theta_JUNC\text{-}CASE}$

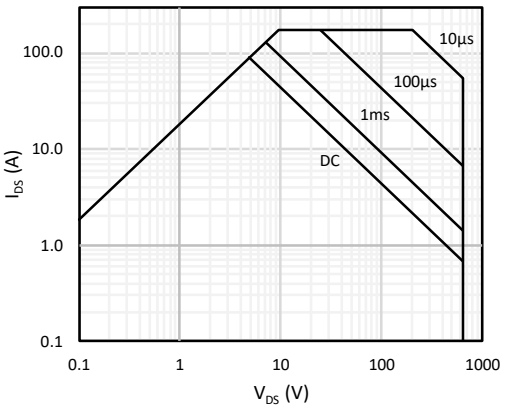
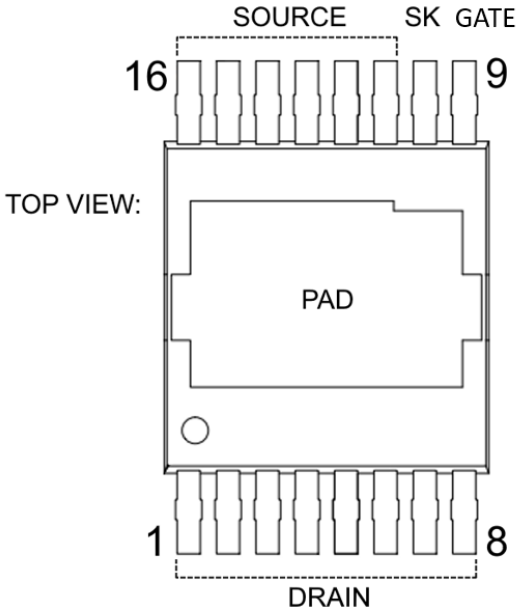


Fig. 14. Safe Operating Area, T_{CASE} = 25°C

11. Pinout Table



Pin		I/O (Note 8)	Description
Number	Symbol		
Top Pad	Source	G	Source of power FET and Thermal Pad for Heatsink
11-16	Source	G	Source of power FET
10	SK	G	Kevlin sense of FET source. Use for driver connection
9	Gate	I	Gate of power FET
1-8	Drain	P	Drain of power FET

(8) G = Ground, I = Input, P = Power

12. Functional Description

12.1. Design for $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

GaN-FETs have been designed and tested to provide significant design margin for continuous and transient voltage conditions, for topologies typically used in high power operation up to 22kW. These voltage levels and recommended design margin can be analyzed using Fig. 15 below. When the switch is turned off, energy stored in the output circuit causes V_{DS} overshoot (V_{SPIKE}), and after dissipation of the stored energy V_{DS} settles to the level of the bus voltage.

- For ***repetitive*** events, derating should be applied from $V_{DS(TRAN)}$ rating (800V) to $V_{DS(CONT)}$ rating (650V max) under the worst case operating conditions.
- It is recommended to design the system such that V_{DS-OFF} is $\leq$ 520V (80% of $V_{DS(CONT)}$ rating).
- ***Non-repetitive events*** are infrequent, ***one-time*** conditions such as line surge, ESD, and lightning strike. No derating from 800V is needed for non-repetitive V_{SPIKE} durations < 100 µs.

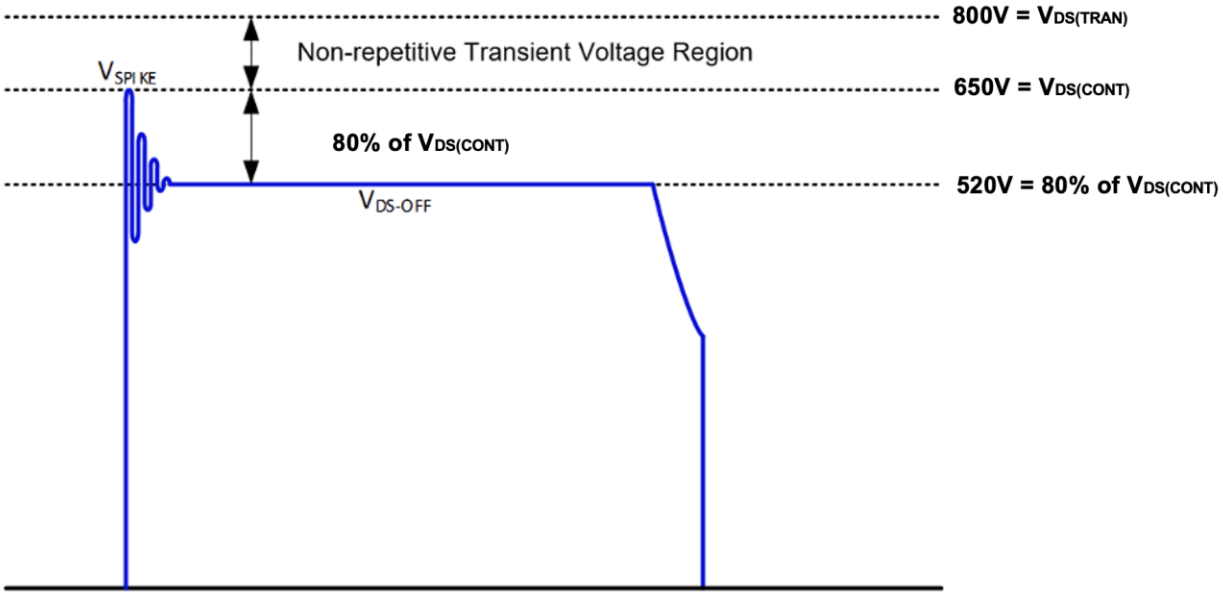
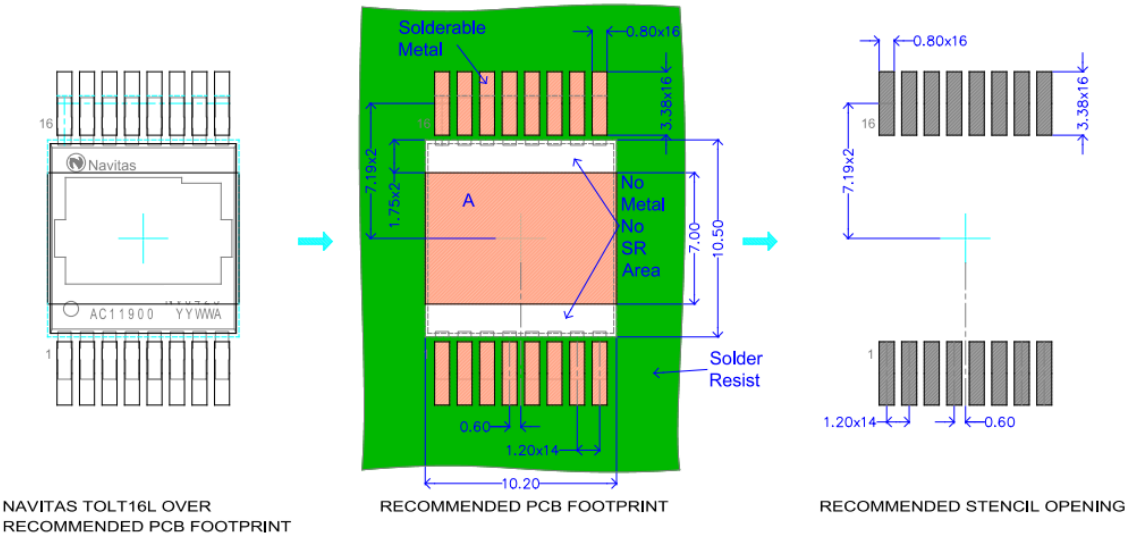


Fig. 15. $V_{DS(CONT)}$ and $V_{DS(TRAN)}$

12.2. PCB Layout Guidelines and PCB Footprint

PCB layout is critical for thermal management, noise immunity, and proper operation of the part. The following rules should be followed carefully during the design of the PCB layout:

- Place IC filter and programming components **directly adjacent to the part**, and reference all these components to the SK pin.
- Place an 0402 site for MLCC between SK and Gate Pins (**directly adjacent to the pins**). This site may be stuffed with a 47pF MLCC if additional noise immunity on Gate Pin is desired.
- Do ***not*** run power SOURCE currents through SK pin!
- System-level thermal design for top-cooled packages must observe co-planarity and electrical isolation requirements when multiple power devices are cooled by the same heatsink (Cold Plate), however, GaN-FET TOLT employs negative offset gull-wing leads to help achieve thermal pad co-planarity across multiple devices. Also, while the majority of heat is transferred thru the top-side thermal pad, placing a Cu Plane below the package (shown below) also transfers heat to the board.

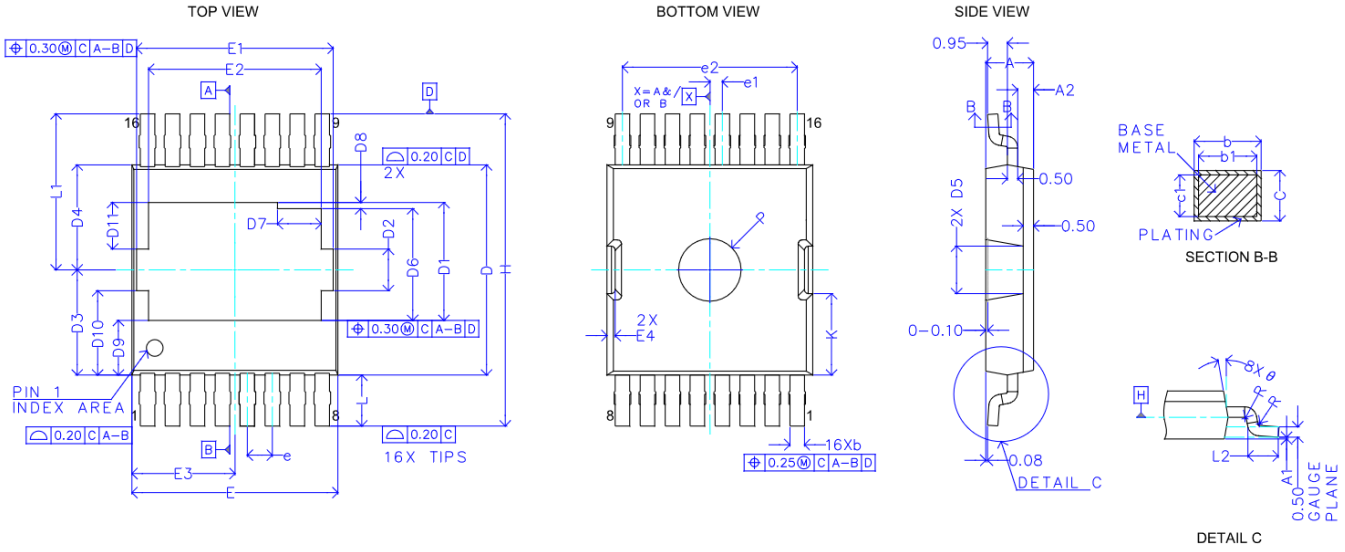


NAVITAS TOLT16L OVER RECOMMENDED PCB FOOTPRINT

RECOMMENDED PCB FOOTPRINT

RECOMMENDED STENCIL OPENING

13. Package Outline Dimensions:



SYMBOL	MIN	MAX	SYMBOL	MIN	MAX
A	2.25	2.35	E	9.70	10.10
A1 (+)	0.01	0.11	E1	9.26	9.66
A2	0.56	0.96	E2	8.10	8.50
b	0.60	0.85	E3	4.75	5.15
b1	0.60	0.80	E4	0.20	0.60
c	0.45	0.65	e	1.20 BSC	
c1	0.45	0.60	e1	0.60 BSC	
D	10.00	10.30	e2	8.40 BSC	
D1	5.47	5.87	H	14.80	15.20
D2	1.80	2.20	K	3.71	4.11
D3	4.85	5.25	L	2.25	2.65
D4	5.00	5.13	L1	7.30	7.70
D5	2.08	2.48	L2	1.30	1.70
D6	5.17	5.57	R	0.07	-
D7	1.80	2.20	P	2.90	3.10
D8	0.10	0.50	θ	4°	10°
D9	2.42	2.82			
D10	3.85	4.25			
D11	2.04	2.44			

14. Revision History

Date	Status	Notes
Sept 22nd, 2025	Preliminary	• First Preliminary Datasheet Publication
Oct 15th, 2025	Preliminary	• Updated I_{GSS} typical
Oct 23rd, 2025	Preliminary	• Added simplified diagram, updated min V_{GS}

Additional Information

EXCEPT TO THE EXTENT THAT INFORMATION IN THIS DATA SHEET IS EXPRESSLY AND SPECIFICALLY WARRANTED IN WRITING BY NAVITAS SEMICONDUCTOR ("NAVITAS"), EITHER PURSUANT TO THE TERMS AND CONDITIONS OF THE LIMITED WARRANTY CONTAINED IN NAVITAS' STANDARD TERMS AND CONDITIONS OF SALE OR A WRITTEN AGREEMENT SIGNED BY AN AUTHORIZED NAVITAS REPRESENTATIVE, (1) ALL INFORMATION IN THIS DATA SHEET OR OTHER DESIGN RESOURCES PROVIDED BY NAVITAS, INCLUDING WITHOUT LIMITATION RELIABILITY AND TECHNICAL DATA, REFERENCE DESIGNS, APPLICATION ADVICE OR TOOLS, AND SAFETY INFORMATION (COLLECTIVELY, "DESIGN RESOURCES"), ARE PROVIDED "AS IS" AND WITH ALL FAULTS; AND (2) NAVITAS MAKES NO WARRANTIES OR REPRESENTATIONS AS TO ANY SUCH INFORMATION OR DESIGN RESOURCES AND HEREBY DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

CUSTOMER RESPONSIBILITIES. This data sheet and other Design Resources provided by Navitas are intended only for technically trained and skilled developers designing with Navitas- or GeneSiC-branded products ("Products"). Performance specifications and the operating parameters of Products described herein are determined in the independent state and may not perform the same way when installed in customer products. The customer (or other user of this data sheet) is solely responsible for (a) designing, validating and testing the application, products and systems in which Products are incorporated; (b) evaluating the suitability of Products for the intended application and the completeness of the information in this data sheet with respect to such application; (c) ensuring the application meets applicable standards and any safety, security, regulatory or other requirements; (d) procuring and/or developing production firmware, if applicable; and (e) completing system qualification, compliance and safety testing, EMC testing, and any automotive, high-reliability or other system qualifications that apply.

NON-AUTHORIZED USES OF PRODUCTS. Except to the extent expressly provided in a writing signed by an authorized Navitas representative, Products are not designed, authorized or warranted for use in extreme or hazardous conditions; aircraft navigation, communication or control systems; aircraft power and propulsion systems; air traffic control systems; military, weapons, space-based or nuclear applications; life-support devices or systems, including but not limited to devices implanted into the human body and emergency medical equipment; or applications where product failure could lead to death, personal injury or severe property or environmental damage. The customer or other persons using Products in such applications without Navitas' agreement or acknowledgement, as set forth in a writing signed by an authorized Navitas representative, do so entirely at their own risk and agree to fully indemnify Navitas for any damages resulting from such improper use.

CHANGES TO, AND USE OF, THIS DATA SHEET. This data sheet and accompanying information and resources are subject to change without notice. Navitas grants you permission to use this data sheet and accompanying resources only for the development of an application that uses the Products described herein and subject to the notices and disclaimers above. Any other use, reproduction or display of this data sheet or accompanying resources and information is prohibited. No license is granted to any Navitas intellectual property right or to any third-party intellectual property right.

TERMS AND CONDITIONS. All purchases and sales of Products are subject to Navitas' Standard Terms and Conditions of Sale, including the limited warranty contained therein, unless other terms and conditions have been agreed in a writing signed by an authorized Navitas representative. This data sheet, and Navitas' provision of this data sheet or other information and resources, do not expand or otherwise alter those terms and conditions.

Navitas, GeneSiC, the Navitas and GeneSiC logos, GaNFast, GaNSafe and other Navitas marks used herein are trademarks or registered trademarks of Navitas Semiconductor Limited or its affiliates. Other trademarks used herein are the property of their respective owners.

Copyright © 2025 Navitas Semiconductor Limited and affiliates. All rights reserved.