# GaNFast™ Power FET

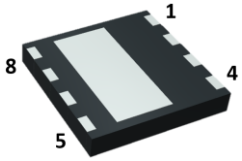
## 1. Features

### GaNFast™ Power IC

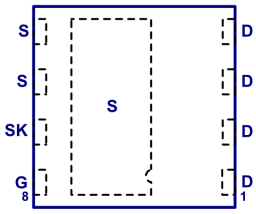
- eMode GaN power FET
- Low 150 mΩ resistance
- 10 MHz switching frequency capability
- Ultra-low gate charge
- Zero reverse recovery charge
- Low output charge
- 900 V Transient Voltage Rating
- Source Kelvin (SK) pin for gate noise immunity
- Small, low-profile SMT DFN
- 8x8 mm PCB footprint
- Minimized package inductance
- Low thermal resistance
- Bottom-side cooled

### Environmental

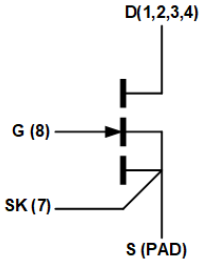
- RoHS, Pb-free, REACH-compliant




PDFN 8x8 mm




Package Outline (Top View)




Simplified Schematic

## 2. Topologies / Applications

- AC-DC, DC-DC, DC-AC
- QR flyback, ACF, buck, boost, half bridge, full bridge, LLC resonant, Class D, PFC
- Wireless power
- LED lighting
- Solar Micro-inverters
- TV SMPS
- Server, Telecom

## 3. Description

This GaNFast™ power FET is a high performance eMode GaN FET that achieves excellent high-frequency and high efficiency operation. Features include a simple gate input and a Source Kelvin pin for noise immunity.

This GaN power FET combines the highest dV/dt immunity and industry-standard low-profile, low-inductance, bottom-side cooled SMT DFN packaging to enable designers to achieve simple, quick and reliable solutions.

Navitas' GaN technology extends the capabilities of traditional topologies such as flyback, half-bridge, buck/boost, LLC and other resonant converters to reach MHz+ frequencies with very high efficiencies and low EMI to achieve unprecedented power densities at a very attractive cost structure.

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# 5. Specifications

## 5.1. Absolute Maximum Ratings(1)

(with respect to Source (pad) unless noted)

| SYMBOL | PARAMETER | MAX | UNITS |
|---|---|---|---|
| $V_{DS(TRAN)}$ | Transient Drain-to-Source Voltage(2) | 900 | V |
| $V_{GS}$ | Continuous Gate-to-Source Voltage | -10 to +7 | V |
| $V_{TGS}$ | Transient Gate-to-Source Voltage(3) | -20 to +10 | V |
| $I_D$ | Continuous Drain Current (@ $T_C$ = 25ºC) | 11 | A |
| $I_D$ | Continuous Drain Current (@ $T_C$ = 100ºC) | 7 | A |
| $I_D$ PULSE | Pulsed Drain Current (10 µs @ $T_J$ = 25°C) | 20 | A |
| dV/dt | Slew Rate on Drain-to-Source | 200 | V/ns |
| $T_J$ | Operating Junction Temperature | -55 to 150 | ºC |
| $T_{STOR}$ | Storage Temperature | -55 to 150 | ºC |

*(1) Absolute maximum ratings are stress ratings; devices subjected to stresses beyond these ratings may cause permanent damage.*

*(2) $V_{DS\ (TRAN)}$ rating allows for surge ratings during non-repetitive events that are < 100us (for example start-up, line interruption). $V_{DS\ (TRAN)}$ rating allows for repetitive events that are < 100ns, with 80% derating required (for example repetitive leakage inductance spikes). Refer to Section 7 for detailed recommended design guidelines.*

*(3) < 1 µsec*

## 5.2. Thermal Resistance

| SYMBOL | PARAMETER | TYP | UNITS |
|---|---|---|---|
| $R_{\theta JC}$ (4) | Junction-to-Case | 1.3 | ºC/W |
| $R_{\theta JA}$ (4) | Junction-to-Ambient | 35 | ºC/W |

*(4) $R_\theta$ measured on DUT mounted on 1 square inch 2 oz Cu (FR4 PCB)*

## 5.3. Electrical Characteristics

Typical conditions: $V_{DS}$ = 400 V, $F_{SW}$ = 1 MHz, $T_{AMB}$ = 25 ºC, $I_D$ = 4 A (or specified)

| SYMBOL | PARAMETER | MIN | TYP | MAX | UNITS | CONDITIONS |
|---|---|---|---|---|---|---|
| GaN FET Characteristics | | | | | | |
| $I_{GSS}$ | Gate-Source Leakage Current | | 35 | | µA | $V_{GS}$ = 6 V |
| $R_{DS(ON)}$ | Drain-Source Resistance | | 150 | 210 | mΩ | $V_{GS}$ = 6 V, $I_D$ = 4 A, $T_J$ = 25 ºC |
| $R_{DS(ON)}$ | Drain-Source Resistance | | 345 | | mΩ | $V_{GS}$ = 6 V, $I_D$ = 4 A, $T_J$ = 150 ºC |
| $V_{GS(th)}$ | Gate Threshold Voltage | 1 | 1.7 | 2.6 | V | $I_D$ = 7 mA, $V_{DS}$ = 0.1 V |
| $V_{SD}$ | Source-Drain Reverse Voltage | | 3.2 | 5 | V | $V_{GS}$ = 0 V, $I_{SD}$ = 4 A |
| $Q_{RR}$ | Reverse Recovery Charge | | 0 | | nC | |
| $R_G$ | Internal Gate Resistance | | 1.6 | | Ω | |
| $C_{ISS}$ | Input Capacitance | | 74 | | pF | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V |
| $C_{OSS}$ | Output Capacitance | | 21 | | pF | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V |
| $C_{RSS}$ | Reverse Transfer Capacitance | | 0.2 | | pF | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V |
| $Q_G$ | Total Gate Charge | | 2.4 | | nC | $V_{GS}$ = 0-6 V, $I_D$ = 8 A, $V_{DS}$ = 400 V |
| $Q_{GD}$ | Gate-to-Drain Charge | | 1.0 | | nC | $V_{GS}$ = 0-6 V, $I_D$ = 8 A, $V_{DS}$ = 400 V |
| $Q_{GS}$ | Gate-to-Source Charge | | 0.5 | | nC | $V_{GS}$ = 0-6 V, $I_D$ = 8 A, $V_{DS}$ = 400 V |
| $Q_{OSS}$ | Output Charge | | 15 | | nC | $V_{GS}$ = 0 V, $V_{DS}$ = 400 V |
| $C_{O(er)}$ (5) | Effective Output Capacitance, Energy Related | | 26 | | pF | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V |
| $C_{O(tr)}$ (6) | Effective Output Capacitance, Time Related | | 38 | | pF | $V_{DS}$ = 400 V, $V_{GS}$ = 0 V |

*(5) $C_{O(er)}$ is a fixed capacitance that gives the same stored energy as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

*(6) $C_{O(tr)}$ is a fixed capacitance that gives the same charging time as $C_{OSS}$ while $V_{DS}$ is rising from 0 to 400 V*

## 5.4. Characteristic Graphs

(GaN FET, $T_C$ = 25 ºC unless otherwise specified)

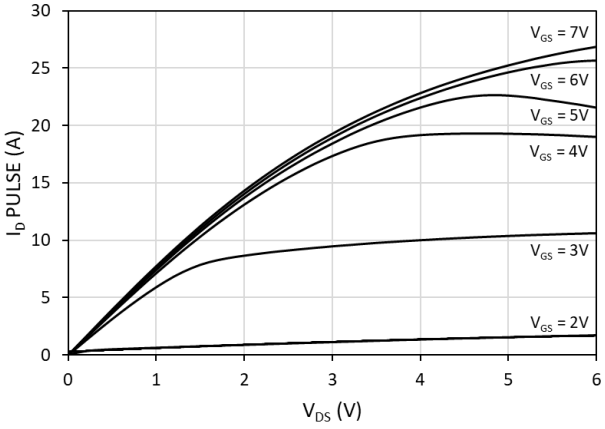



Fig. 1 Pulsed drain current ($I_D$ PULSE) vs. drain-to-source voltage ($V_{DS}$) at T = 25 °C

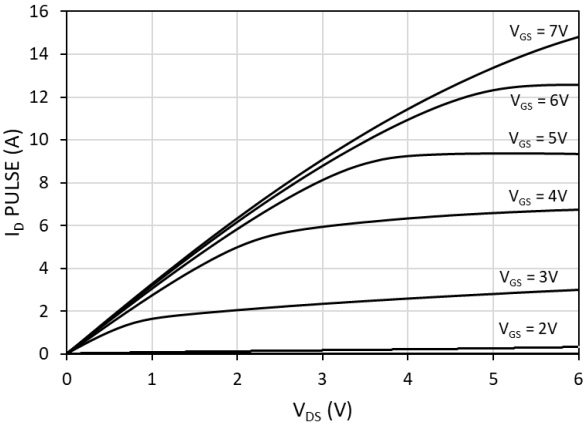



Fig. 2 Pulsed drain current ($I_D$ PULSE) vs. drain-to-source voltage ($V_{DS}$) at T = 150 °C

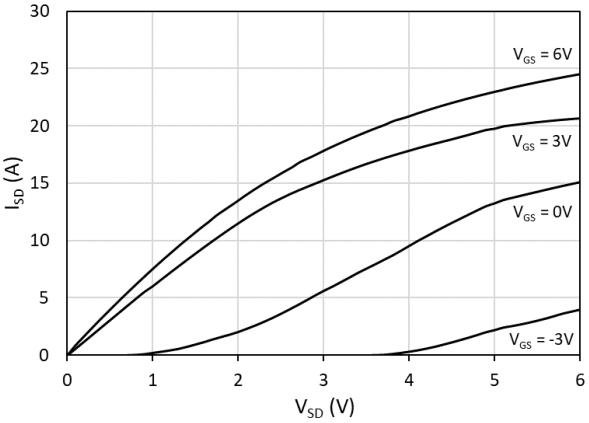



Fig. 3 Source-to-drain reverse conduction voltage at T = 25 °C

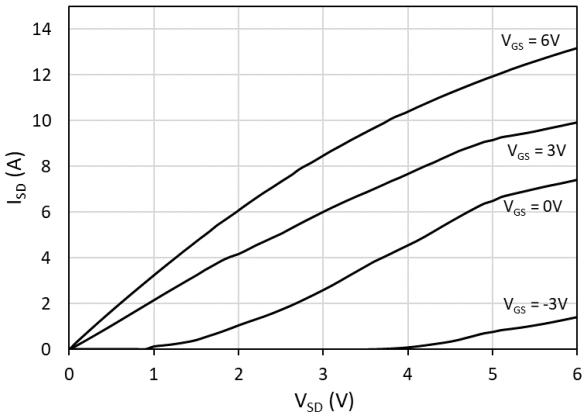



Fig. 4 Source-to-drain reverse conduction voltage at T = 150 °C

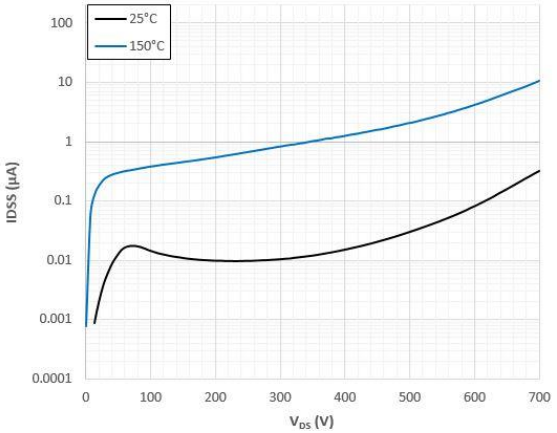



Fig. 5 Drain-to-source leakage current ($I_{DSS}$) vs. drain-to-source voltage ($V_{DS}$)

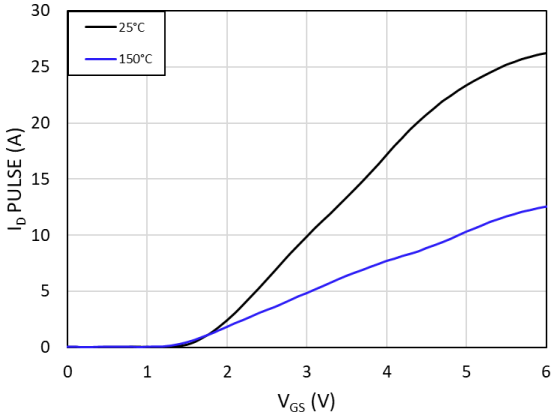



Fig. 6 Pulsed drain current ($I_D$ PULSE) vs. gate-to-source voltage ($V_{GS}$)

## Characteristic Graphs (Cont.)

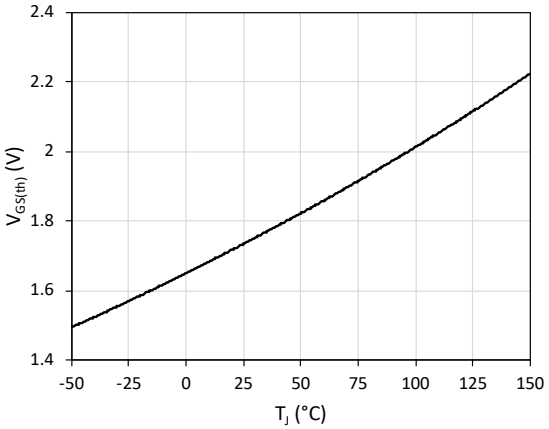



Fig. 7 Gate threshold voltage ($V_{GS(th)}$) vs. junction temperature ($T_J$)

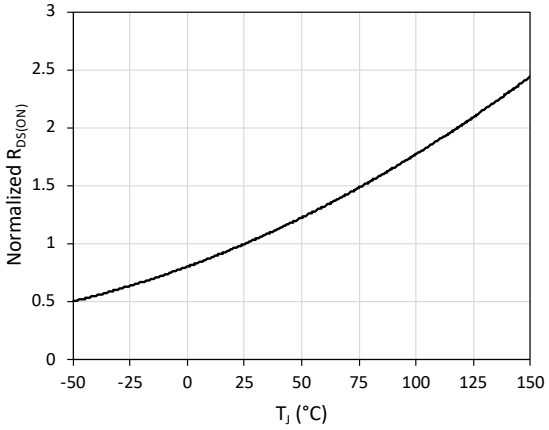



Fig. 8 Normalized on-resistance ($R_{DS(ON)}$) vs. junction temperature ($T_J$)

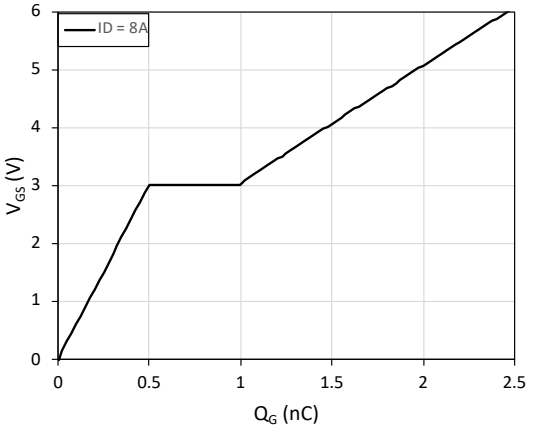



Fig. 9 Gate-to-source voltage ($V_{GS}$) vs. total gate Charge ($Q_G$)

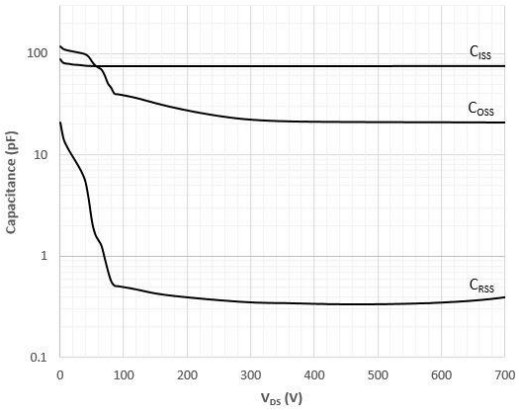



Fig. 10 Input Capacitance ($C_{ISS}$), Output capacitance ($C_{OSS}$), Reverse Transfer capacitance ($C_{RSS}$), vs. drain-to-source voltage ($V_{DS}$)

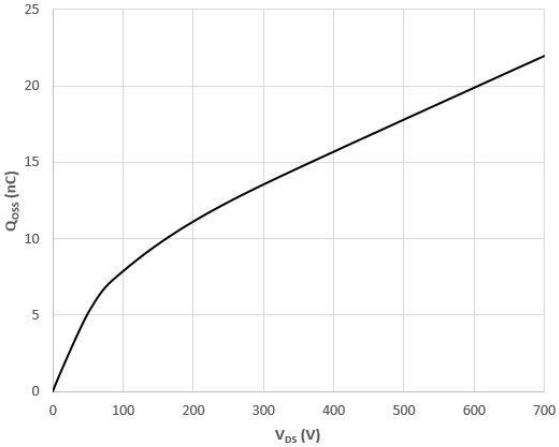



Fig. 11 Charge stored in output capacitance ($Q_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)

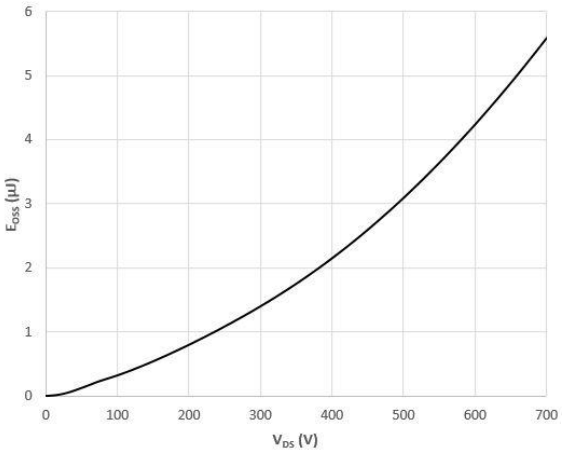



Fig. 12 Energy stored in output capacitance ($E_{OSS}$) vs. drain-to-source voltage ($V_{DS}$)

## Characteristic Graphs (Cont.)

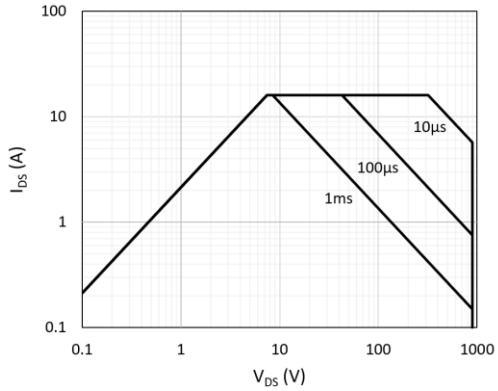



Fig. 13 SOA @ Tcase = 25ºC

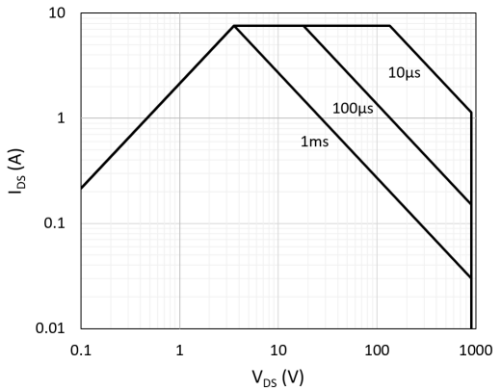
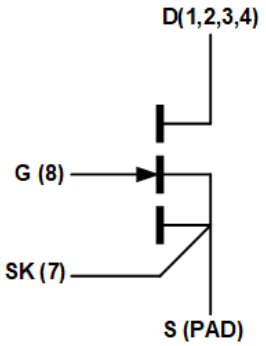
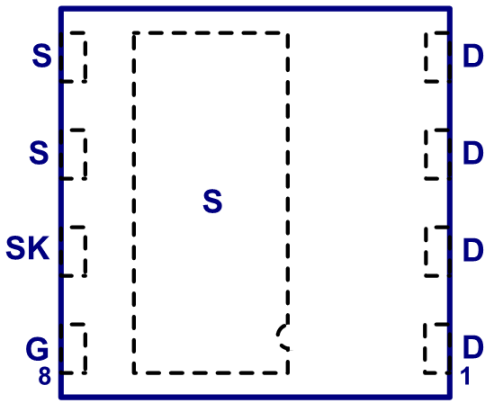



Fig. 14 SOA @ Tcase = 125ºC

## 6. Pin Configurations and Functions




Package Top View

| Pin Number | Pin Name | Description |
|---|---|---|
| 5, 6 | NC | No connection, leave floating or connect to Source PAD |
| 7 | SK | Kelvin sense of FET source. Use for driver connection |
| 8 | G | Gate of power FET |
| 1, 2, 3, 4 | D | Drain of power FET |
| PAD | S | Source of power FET. Metal pad on bottom of package. |

## 7. Drain-to-Source Voltage Considerations

GaN Power ICs have been designed and tested to provide significant design margin to handle transient and continuous voltage conditions that are commonly seen in single-ended topologies, such as quasi-resonant (QR) flyback applications. The different voltage levels and recommended margins in a typical QR flyback can be analyzed using Fig. 15. When the device is switched off, the energy stored in the transformer leakage inductance will cause $V_{DS}$ to overshoot to the level of $V_{SPIKE}$. The clamp circuit should be designed to control the magnitude of $V_{SPIKE}$. After dissipation of the leakage energy, the device $V_{DS}$ will settle to the level of the bus voltage plus the reflected output voltage which is defined in Fig. 15 as $V_{DS-OFF}$.

- For repetitive events, 80% derating should be applied from $V_{DS\ (TRAN)}$ rating (900V) to 720V max under the worst case operating conditions.
- It is recommended to design the system such that $V_{DS-OFF}$ < 560V.
- Non-repetitive events are infrequent, one-time conditions such as line surge, ESD, and lightning. No derating from the $V_{DS(TRAN)}$ rating (900V) is needed for non-repetitive $V_{SPIKE}$ durations < 100 µs. The $V_{DS(TRAN)}$ rating (900V) allows for repetitive events that are <100ns, with 80% derating required (for example repetitive leakage inductance spikes).

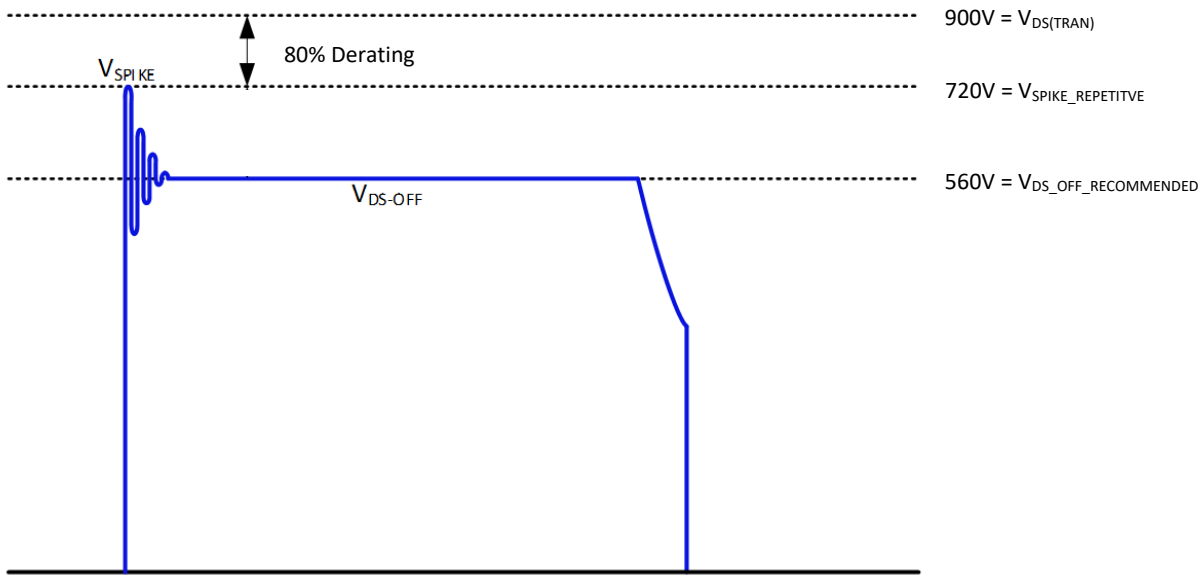
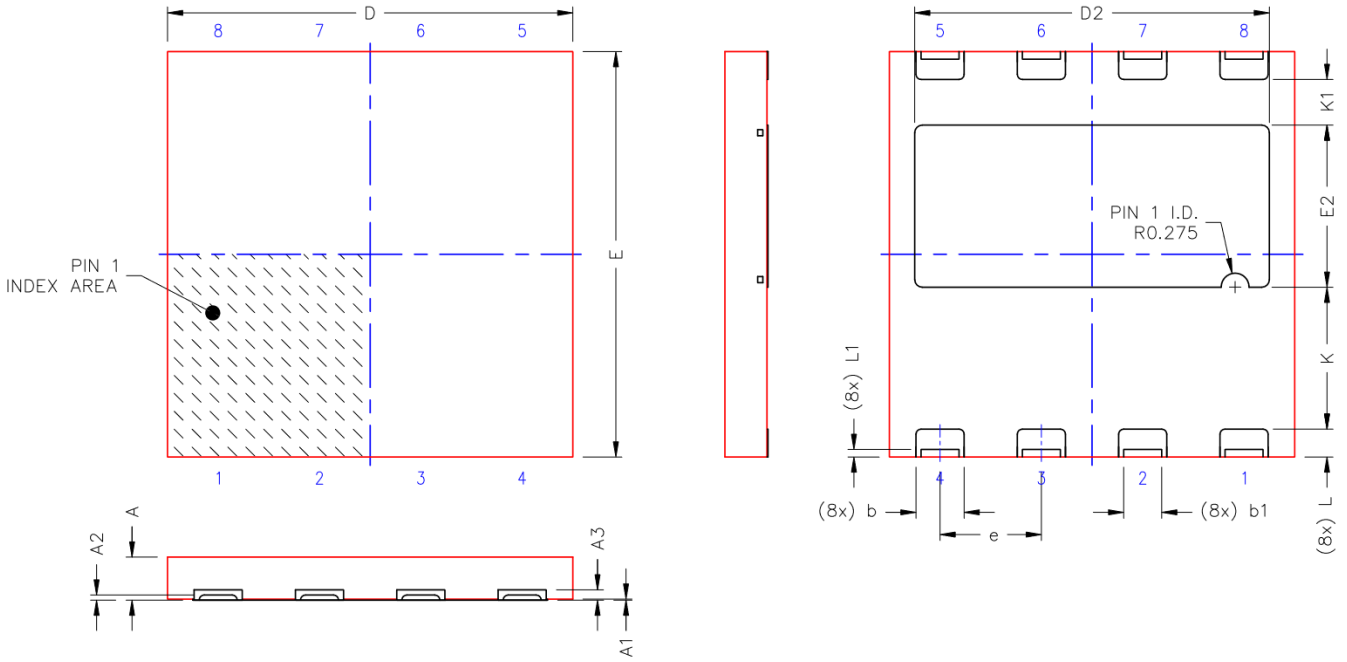



Fig. 15. QR flyback drain-to-source voltage stress diagram

## 8. PDFN Package Outline




| SYM | MIN | NOM | MAX |
|---|---|---|---|
| A | 0.80 | 0.85 | 0.90 |
| A1 | 0.00 | – | 0.05 |
| A2 | – | 0.102 REF. | – |
| A3 | – | 0.203 REF. | – |
| b | 0.90 | 0.95 | 1.00 |
| b1 | – | 0.75 REF. | – |
| D | 7.90 | 8.00 | 8.10 |
| D2 | 6.95 | 7.00 | 7.05 |
| E | 7.90 | 8.00 | 8.10 |
| E2 | 3.15 | 3.20 | 3.25 |
| e | | 2.00 TYP. | |
| K | – | 2.80 REF. | – |
| K1 | – | 0.90 REF. | – |
| L | 0.50 | 0.55 | 0.60 |
| L1 | – | 0.15 REF. | – |

NOTES:

1. DIMENSIONING AND TOLERANCING CONFORM TO ASME Y14.5M – 1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS.
3. MAXIMUM ALLOWABLE BURRS IS 0.050 MM IN ALL DIRECTIONS.

## 9. Ordering Information

| Part Number | Operating Temperature Grade | Storage Temperature Range | Package | MSL Rating | Packing (Tape & Reel) |
|---|---|---|---|---|---|
| NV6026C-RA | -55 °C to +150 °C $T_{CASE}$ | -55 °C to +150 °C $T_{CASE}$ | 8 x 8 mm DFN | 3 | 1,000 : 7” Reel |
| NV6026C | -55 °C to +150 °C $T_{CASE}$ | -55 °C to +150 °C $T_{CASE}$ | 8 x 8 mm DFN | 3 | 3,000 : 13” Reel |

## 10. Revision History

| Date | Status | Notes |
|---|---|---|
| Nov 18, 2024 | FINAL | First Publication |
| Mar 3, 2025 | FINAL | Remove VDSmax(cont) rating, remove IDSS ratings, add SOA curves |

## Additional Information

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