# E-mode vs. D-mode GaN: What the Cascode Si FET Costs You

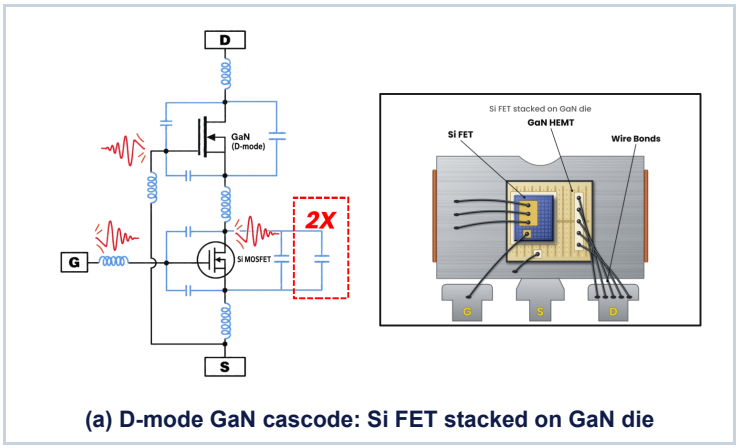
An evaluation of complexity, parasitics, and switching figures of merit to determine the best GaN technology

Two device structures dominate 650 V GaN power switching. Depletion-mode (D-mode) GaN is normally on, so it is paired with a low-voltage silicon MOSFET in a cascode to create a normally-off switch. Enhancement-mode (E-mode) GaN is normally off by itself, so a single monolithic die does the job. This design tip compares the two structures, shows where the cascode Si FET adds parasitics, charge, and complexity, and walks through a datasheet comparison of a Navitas E-mode GaN IC against a close equivalent D-mode cascode device.

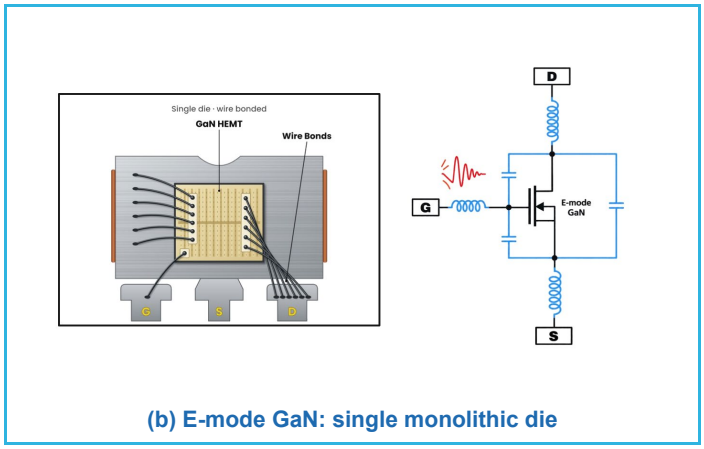
## Two ways to build a normally off GaN switch

In a D-mode cascode, a low-voltage Si MOSFET sits in series with the source of the GaN HEMT, and the HEMT gate is tied to the system source. The designer drives the Si MOSFET, which in turn controls the HEMT. In many packages, the Si FET die is stacked directly on the GaN die and connected with wire bonds (Figure 1a). The approach works, but it adds a second die and extra process steps. It also introduces a network of interacting parasitic inductances and capacitances, as well as an added delay between the two devices.

An E-mode GaN HEMT is off at zero gate bias without any helper device, so a single die is wire-bonded directly to the G, S and D terminals (Figure 1b). With no internal cascode node, there is no added delay or parasitic network, and because the GaN gate is driven directly, switching speed can be set with the gate resistor. The same monolithic process also allows drive, sensing and protection to be integrated on the die, which simplifies the design.




(a) D-mode GaN cascode: Si FET stacked on GaN die




(b) E-mode GaN: single monolithic die

**Figure 1.** *Equivalent circuits and package construction. Red waveforms mark ringing-prone nodes; the dashed 2X box highlights the additional capacitance introduced by the cascode Si MOSFET. Package drawings are representative illustrations [1].*

## Architecture-level comparison

Table 1 summarizes how the two approaches differ at the device level. Most of the D-mode penalties trace back to the same root cause: the extra Si MOSFET and the internal node it creates.

| Criterion | E-mode GaN (e.g., Navitas NV6034) | D-mode cascode |
|---|---|---|
| **Die** | **Monolithic, single die** | Two die (GaN + Si MOSFET), co-packaged |
| **Reverse recovery ($Q_{RR}$)** | **Almost zero (no body diode)** | Si body diode reverse recovery |
| **dV/dt control** | **Set directly by gate resistor** | Indirect; turn-off and ringing hard to tune |
| **Monolithic integration** | **Driver, sensing, protection on-die** | Not practical |
| **Dynamic parameters ($Q_G$, $C_{ISS}$)** | **Very low** | Higher (Si MOSFET adds charge) |
| **Input FOM ($R_{DS(on)}$ × $Q_G$)** | **Very good** | Degraded by Si MOSFET |
| **Output FOM ($R_{DS(on)}$ × $Q_{OSS}$)** | **Very good** | Degraded by Si MOSFET |
| **Cascode FET reliability** | **No cascode FET** | Cascode FET avalanche risk |
| **Soft switching** | **Better (lower $C_{OSS}$, $Q_{OSS}$)** | High-frequency performance suffers |

**Table 1.** *E-mode GaN vs. D-mode cascode GaN, device-level comparison.*

D-mode retains one real advantage: because the designer drives a silicon MOSFET, the cascode is easier to gate drive. In most high-frequency and soft-switching designs, the E-mode gains in switching figures of merit, efficiency, and integration outweigh it.

## Datasheet example: NV6034 E-mode vs. 650 V D-mode GaN with cascoded Si FET

The comparison below uses typical datasheet values for the Navitas NV6034 and a close equivalent 650 V D-mode cascode device, with both in comparable 8x8 mm packages. The NV6034 leads on every charge and capacitance figure of merit by 24% to 61%, with a 15% lower typical $R_{DS(on)}$ and 64% lower top-side thermal resistance.

**55%**
**lower $R_{DS(on)}$ × $Q_{OSS}$ FOM**
Lower $E_{OSS}$ and dead-time losses at MHz and in ZVS (LLC/CLLC) designs

**35%**
**lower $R_{DS(on)}$ × $Q_G$ FOM**
Less energy to drive the gate every cycle

**64%**
**lower top-side $R_{\theta JC}$**
0.13 vs. 0.36°C/W for cooler operation

| Parameter | Unit | 650 V D-mode GaN | 650V Navitas (NV6034) | Navitas advantage |
|---|---|---|---|---|
| $V_{DS}$ min | V | 650 | 650 | — |
| $V_{(TR)DSS}$ max (transient) | V | 900 @ 10 µs | 800 @ 100 µs | — |
| $R_{DS(on)}$ typ | mΩ | 20 | 17 | 15% lower |
| $R_{DS(on)}$ max | mΩ | 25 | 25 | — |
| $V_{th}$ typ | V | 4.0 | 1.5 | — |
| $I_D$ max @ 25 °C | A | 92 | 130 | 41% higher |
| $Q_G$ typ | nC | 19.6 | 14.9 | 24% lower |
| $Q_{OSS}$ | nC | 221 | 118 | 47% lower |
| $R_{DS(on)}$ × $Q_G$ (FOM) | mΩ·nC | 392 | 253 | 35% lower |
| $R_{DS(on)}$ × $Q_{OSS}$ (FOM) | mΩ·nC | 4,420 | 2,006 | 55% lower |
| $C_{ISS}$ typ | pF | 1,439 | 560 | 61% lower |
| $C_{OSS}$ typ | pF | 196 | 136 | 31% lower |
| $R_{\theta JC}$ top side | °C/W | 0.36 | 0.13 | 64% lower |
| Temperature range ($T_J$) | °C | −55 to +150 | −40 to +150 | — |
| Package | — | PQFN 8x8, dual-side cooled, 10 leads | DFN 8x8, top-cooled, 10 pins | — |

**Table 2.** *Datasheet comparison, typical values unless noted. Percentages show the E-mode NV6034 improvement relative to the D-mode device.*

## Design tips

- **Re-tune dead time in ZVS converters.** In LLC and CLLC stages, the 47% lower $Q_{OSS}$ means the resonant current completes the switching transition sooner, so the dead time set for a cascode part can usually be shortened, reducing circulating-current and $E_{OSS}$-related loss at high frequency.
- **Use the gate resistor to set dV/dt.** With direct access to the GaN gate, turn-on and turn-off edges can be shaped with gate resistance instead of fighting ringing at an internal cascode node.
- **Respect the lower threshold.** $V_{th}$ is 1.5 V typical versus 4.0 V for the cascode. Keep the gate loop short, use the Kelvin source connection, and follow the gate-drive recommendations in the data sheet.
- **Plan the thermal path for top-side cooling.** The NV6034 is top-cooled at 0.13 °C/W junction-to-case. When migrating from a dual-side-cooled package, route heat through the top of the package to a heatsink rather than relying on the PCB.
- **Take advantage of zero reverse recovery.** With no body diode, hard-switched half-bridges avoid the $Q_{RR}$ loss and ringing that the cascode Si FET's body diode introduces.

## Conclusion

E-mode GaN ICs drop the cascode Si FET entirely. The result is lower complexity, fewer parasitics, and cleaner switching, with measurable gains in $R_{DS(on)}$ x $Q_G$, $R_{DS(on)}$ x $Q_{OSS}$ and thermal resistance that translate directly into higher efficiency and power density.