2300 V 8 mΩ Full-Bridge Power Module

SiCPAK® Power Module

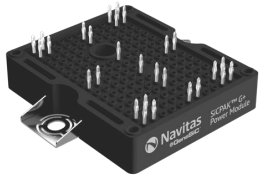
Trench-Assisted Planar SiC MOSFET Technology

V_{DS}	=	2300 V
$R_{DS(ON)}$(Typ.)	=	8.0 mΩ
$I_{D,DC}$ (T_H = 75°C)	=	196 A

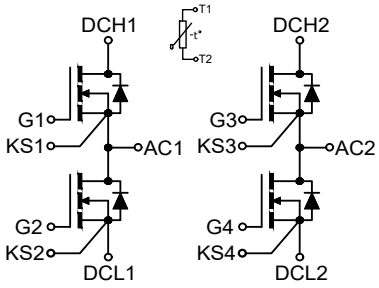
Features

- Epoxy-Resin Potting Technology
- Optimized Package with High Current Press-Fit Pins
- Integrated AlN AMB for >5kV Isolation
- Best-in-Class $R_{DS(ON)}$ over Temperature
- Lower Q_{GD} and Optimized $R_{G(INT)}$
- Best-in-Class Q_{GD}/Q_{GS} and High $V_{GS,th}$
- Optimized Body Diode Snappiness and Low Q_{RR}
- Qualified to Tests Harsher than JEDEC & AEC-Q101

Package



SiCPAK™ G+



Advantages

- Improved Thermal Cycling & Humidity Reliability
- Improved Ampacity & Lower Temperature Rise
- Reduced Coupling Capacitance and Radiated EMI
- Lowest Conduction Losses at all Temperatures
- Faster and More Efficient Switching
- Lower dV/dt Induced Gate Voltage Bounce
- Improved Hard-Switching Performance
- Longer Reliability and Lifetime

Applications

- Data Center Solid State Transformer (SST)
- Battery Energy Storage System (BESS)
- Utility-Scale Solar Optimizer and Inverter
- EV Megawatt Charging System (MCS)
- H2 Fuel Cell Electrolyzer and DC-DC
- Industrial Motor Drive
- High Voltage Power Supply

Absolute Maximum Ratings per MOSFET

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS(max)}$	V_{GS} = 0 V, I_D = 150 µA	2300	V	
Gate-Source Voltage (Transient Maximum)	$V_{GS(tr,max)}$	Transient Pulse Width < 50 ns	-12 / +25	V	
Gate-Source Voltage (Static Maximum)	$V_{GS(max)}$		-10 / +23	V	
Gate-Source Voltage (Static)	$V_{GS(op)-ON}$ $V_{GS(op)-OFF}$	Recommended Operation	+18 to +15 -5 to -3	V	Note 1
DC Continuous Drain Current	$I_{D,DC}$	T_H = 25°C, V_{GS} = -5 / +18 V T_H = 75°C, V_{GS} = -5 / +18 V T_H = 100°C, V_{GS} = -5 / +18 V	239 196 169	A	
Pulsed Drain Current	$I_{D(pulse)}$	t_P ≤ 5µs, D ≤ 1%, V_{GS} = 18 V	350	A	Note 2
Power Dissipation	P_D	T_c = 25°C	2542	W	Fig. 17
Virtual Junction Temperature	$T_{j,ov}$		-55 to 175	°C	
Case Temperature	T_C		-55 to 150	°C	

Note 1: This product can support 0V turn-off gate drive voltage with optimized PCB layout and gate drive circuit configuration.

Note 2: Pulse Width t_P Limited by $T_{j(max)}$

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

SEE IMPORTANT NOTICES AND DISCLAIMERS AT THE END OF THIS DATA SHEET REGARDING THE INFORMATION IN THIS DATA SHEET, THE USE OF OUR PRODUCTS, AND YOUR RESPONSIBILITIES RELATING TO SUCH USE.

Electrical Characteristics per MOSFET (At T_j = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 150 µA	2300			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 2300 V, V_{GS} = 0 V		30	150	µA	
Gate Source Leakage Current	I_{GSS}	V_{DS} = 0 V, V_{GS} = 23 V V_{DS} = 0 V, V_{GS} = -10 V			150 -150	nA	
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 135 mA	2.5	3.2	4.7	V	Note 3
Transconductance	g_{fs}	V_{DS} = 10 V, I_D = 135 A V_{DS} = 10 V, I_D = 135 A, T_j = 175°C		84.9 89.7		S	Fig. 5
Drain-Source On-State Resistance (Die Only)	$R_{DS(ON)}$	V_{GS} = 18 V, I_D = 135 A V_{GS} = 18 V, I_D = 135 A, T_j = 175°C V_{GS} = 15 V, I_D = 135 A V_{GS} = 15 V, I_D = 135 A, T_j = 175°C		8 21 8.9 21.5	10.8	mΩ	Fig. 5-9
Input Capacitance	C_{iss}	V_{DS} = 1500 V, V_{GS} = 0 V f = 100 KHz, V_{AC} = 25mV		21038		pF	Fig. 12
Output Capacitance	C_{oss}			391			
Reverse Transfer Capacitance	C_{rss}			44.5			
C_{oss} Stored Energy	E_{oss}			523		µJ	Fig. 13
C_{oss} Stored Charge	Q_{oss}			1036		nC	
Effective Output Capacitance (Energy Related)	$C_{o(er)}$			465		pF	Note 4
Effective Output Capacitance (Time Related)	$C_{o(tr)}$			691			
Gate-Source Charge	Q_{gs}	V_{DS} = 1500 V, V_{GS} = -5 / +18 V I_D = 135 A Per JEDEC JEP-192		222		nC	Fig. 11
Gate-Drain Charge	Q_{gd}			262			
Total Gate Charge	Q_g			909			
Internal Gate Resistance	$R_{G(int)}$	V_{GS} = 18 V, f = 100 kHz, V_{AC} = 25 mV		0.45		Ω	
Turn-On Switching Energy (FWD = Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+18V, $R_{G,on(ext)}$ = 2 Ω, $R_{G,off(ext)}$= 1 Ω, L = 160.0 µH, I_D= 120 A, V_{DD} = 1500 V		6183		µJ	Fig. 24-26
Turn-Off Switching Energy (FWD = Body Diode)	E_{Off}			724			

Note 3: Tested after applying 30ms pulse at Vgs= +25V

Note 4: $C_{o(er)}$, a lumped capacitance that gives same stored energy as C_{OSS} while V_{DS} is rising from 0 to 1500V.
$C_{o(tr)}$, a lumped capacitance that gives same charging times as C_{OSS} while V_{DS} is rising from 0 to 1500V.

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

MOSFET Body Diode Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	V_{GS} = -5 V, I_{SD} = 67 A		4.1		V	Fig. 18-19
		V_{GS} = -5 V, I_{SD} = 67 A, T_j = 175°C		3.6			
Continuous Diode Forward Current	I_S	V_{GS} = -5 V, T_c = 25°C			359	A	
		V_{GS} = -5 V, T_c = 100°C			223		
Diode Pulse Current	$I_{S(pulse)}$	V_{GS} = -5 V		892		A	Note 2
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 120 A, V_R = 1500 V dif/dt = 21500 A/µs, T_j = 25°C		24		ns	
Reverse Recovery Charge	Q_{rr}			2440		nC	
Peak Reverse Recovery Current	I_{rrm}			176		A	
Reverse Recovery Time	t_{rr}	V_{GS} = -5 V, I_{SD} = 120 A, V_R = 1500 V dif/dt = 21500 A/µs, T_j = 125°C		37		ns	
Reverse Recovery Charge	Q_{rr}			6561		nC	
Peak Reverse Recovery Current	I_{rrm}			334		A	

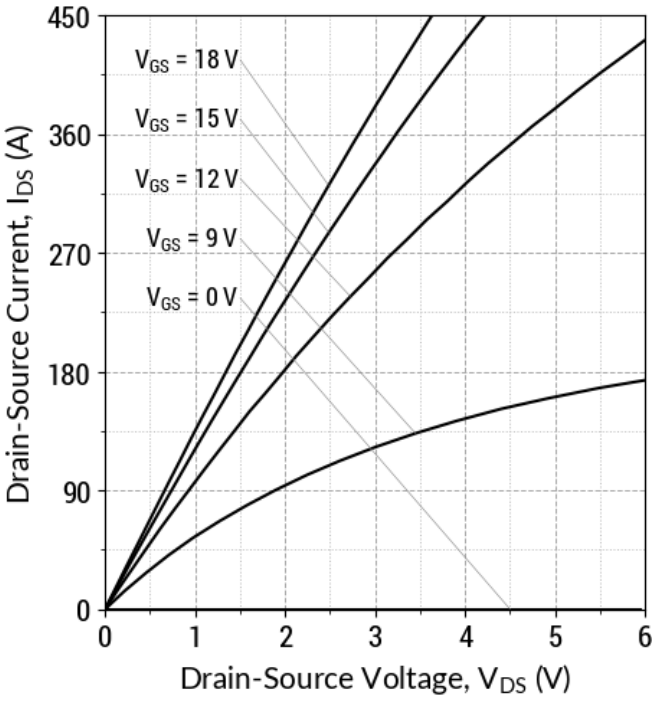
Power Module Characteristics

Parameter	Symbol	Conditions	Values	Unit	Note
Thermal Resistance, Junction - Case (Per Switch, Typical Value)	$R_{th,JC}$	Excludes TIM	0.06	°C/W	Fig. 14
Thermal Resistance, Junction - Heatsink (Per Switch, Typical Value)	$R_{th,JHS}$	110 µm, 4.4 W/m.K	0.114	°C/W	
Weight	W_T		50	g	
Internal Isolation		Basic Insulation	AlN		
Minimum Case Isolation Voltage	V_{ISO}	AC, 50 Hz, 1 Minute	5000	V	
Comparative Tracking Index	CTI	Minimum	600		
Stray Inductance	L_{Stray}	Between DC+ & DC-, 10 MHz	12.40	nH	Half-Bridge
Package Resistane, HS	$R_{PKG,HS}$	T_C = 25°C	1.85	mΩ	Half-Bridge
Package Resistance, LS	$R_{PKG,LS}$	T_C = 25°C	1.95	mΩ	Half-Bridge
Creepage Distance		Terminal to Terminal	9.6	mm	
		Terminal to Heatsink	17.1	mm	
Clearance Distance		Terminal to Terminal	9.6	mm	
		Terminal to Heatsink	13.2	mm	

NTC-Thermistor Characteristics

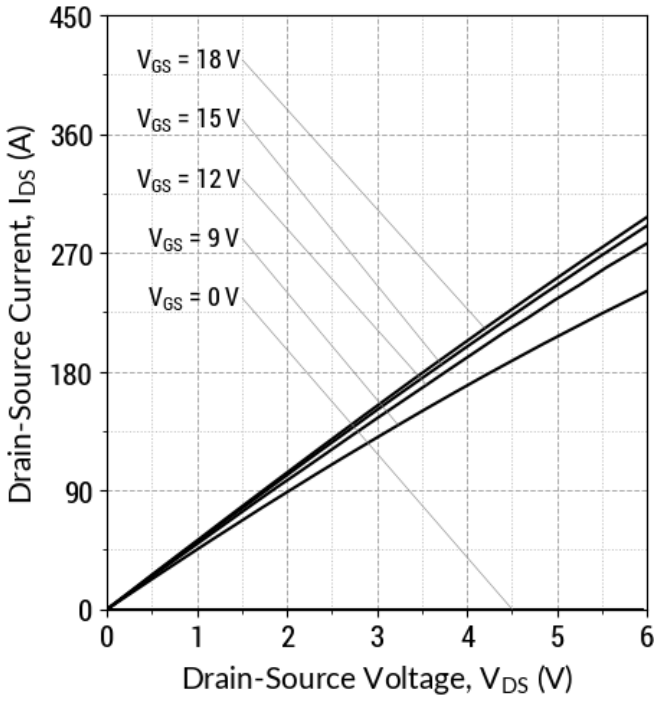
Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Rated Resistance	$R_{NTC,25}$	T_{NTC} = 25 °C		5		kΩ	
Resistance Tolerance	ΔR/R	T_{NTC} = 25 °C	-3		+3	%	
Power Dissipation	$P_{NTC,25}$	T_{NTC} = 25 °C			20	mW	
Beta Value (B-value)	B_{25}/B_{50}	T_2 = 50 °C		3375		K	
	B_{25}/B_{80}	T_2 = 80 °C		3410			
	B_{25}/B_{100}	T_2 = 100 °C		3435			

Fig 1: Typical Output Characteristics (T_j = 25°C)



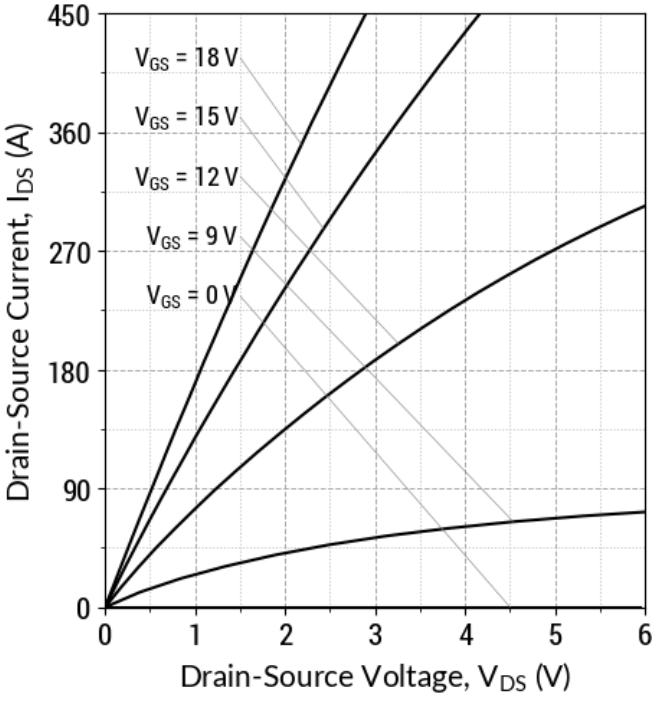
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 2: Typical Output Characteristics (T_j = 175°C)



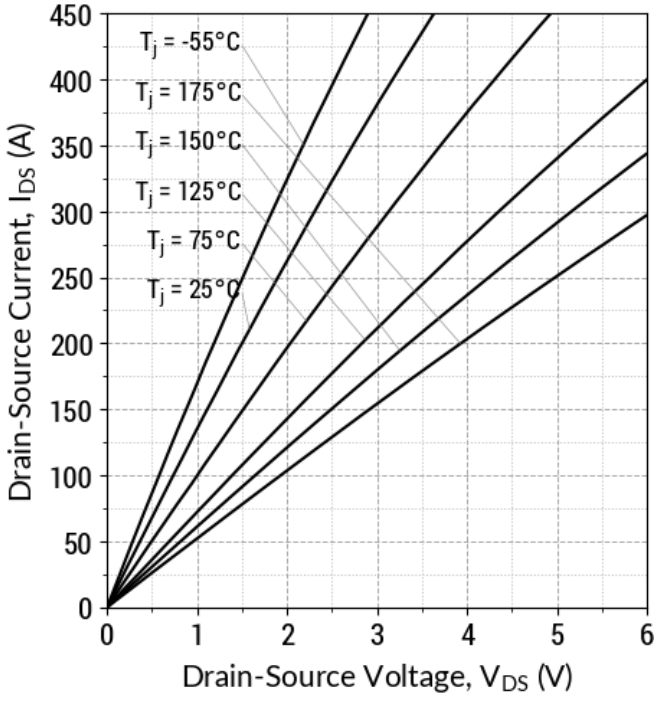
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 3: Typical Output Characteristics (T_j = -55°C)



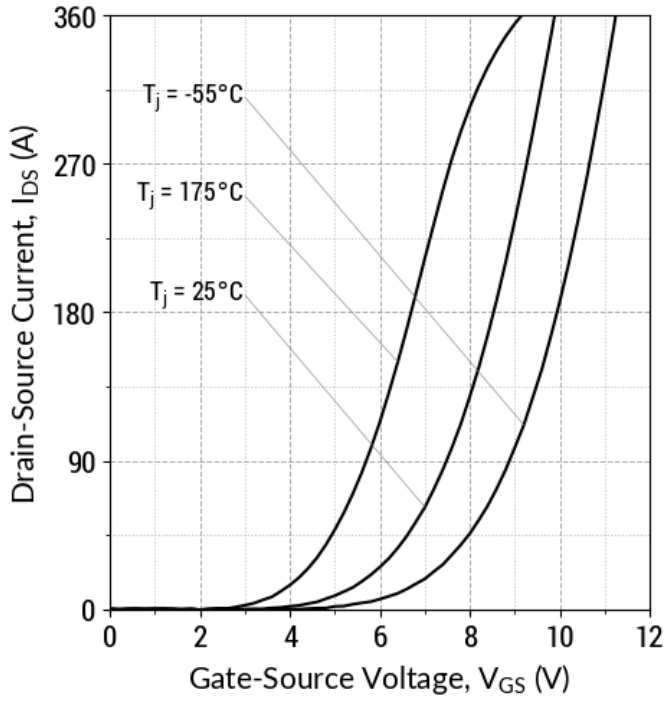
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



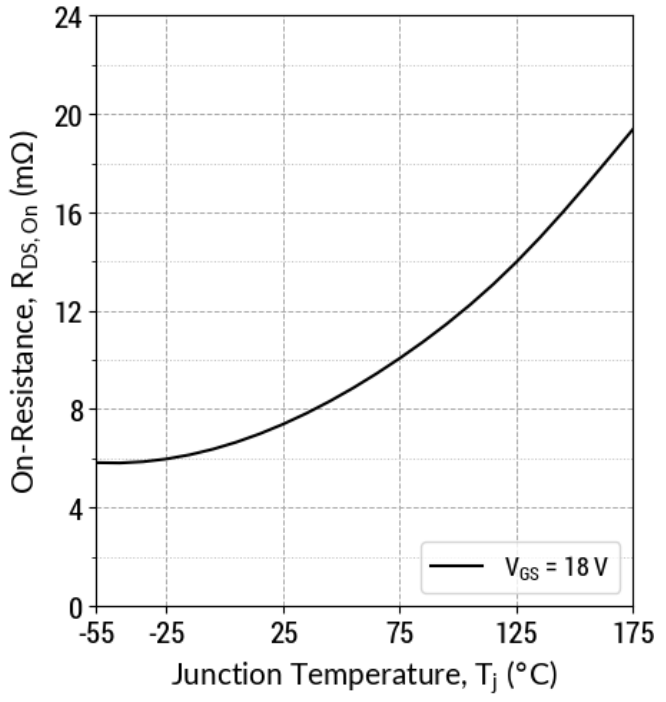
$I_D = f(V_{DS}, T_j)$; t_P = 50 µs

Fig 5: Typical Transfer Characteristics (V_{DS} = 10 V)



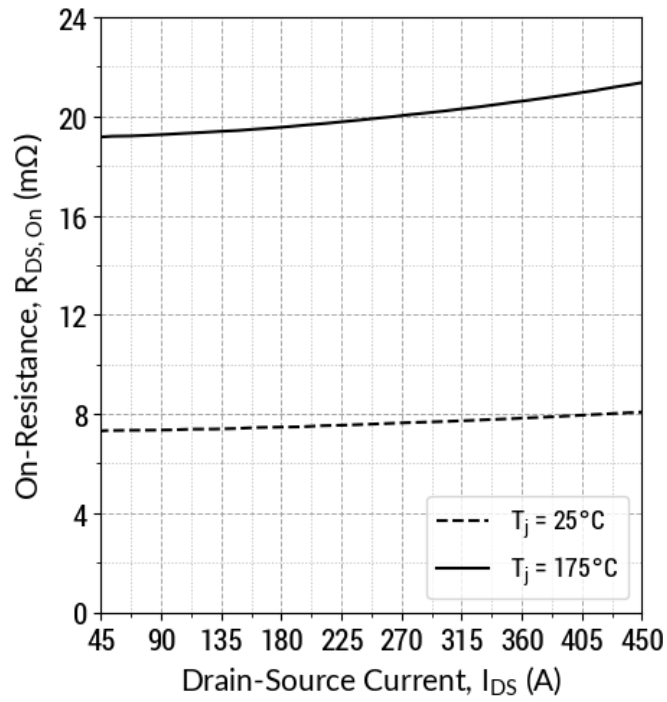
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature



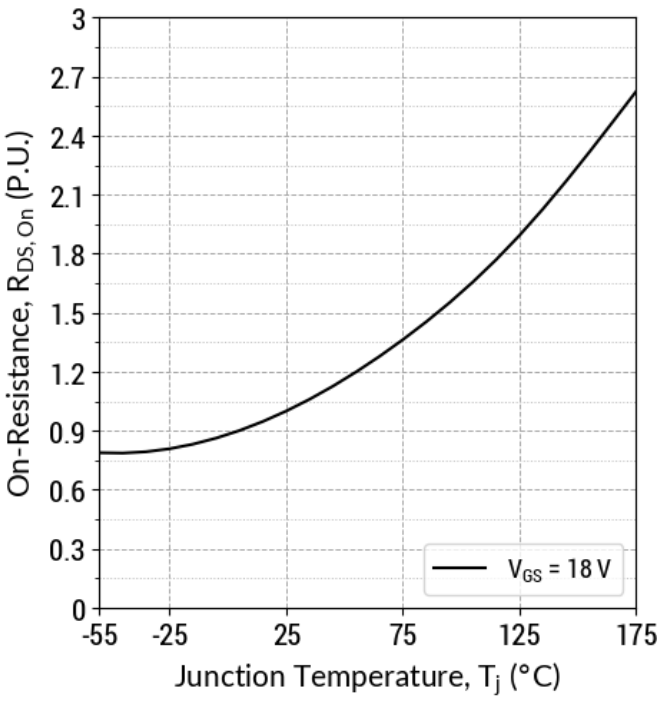
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 135 A

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current



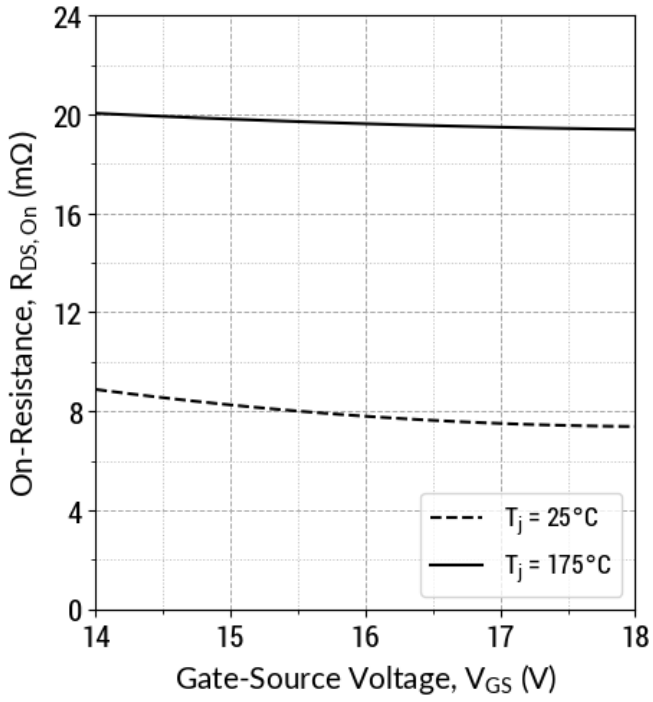
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 50 µs; V_{GS} = 18 V

Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature



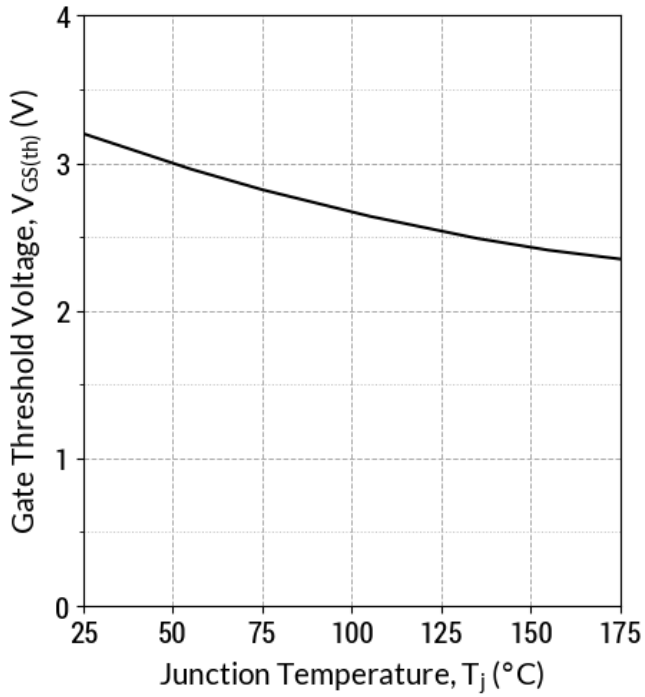
$R_{DS(ON)} = f(T_j)$; t_P = 50 µs; I_D = 135 A

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage



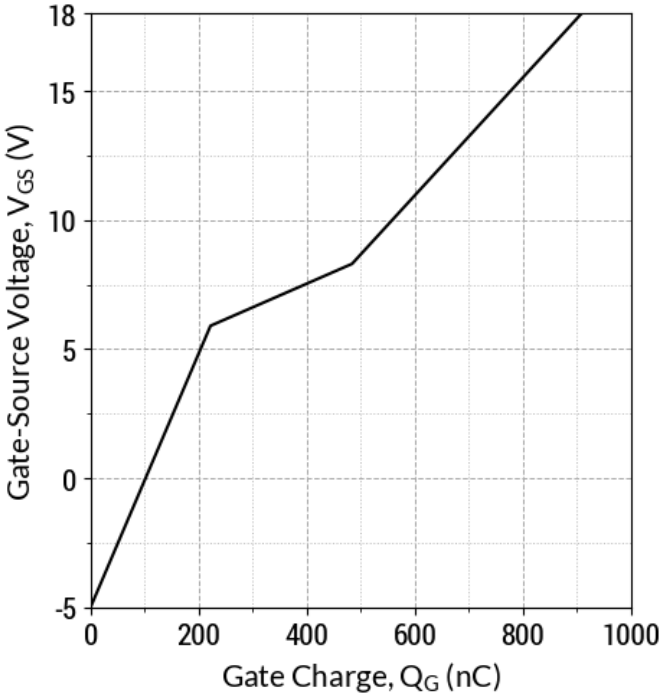
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 135 A

Fig 10: Typical Threshold Voltage Characteristics



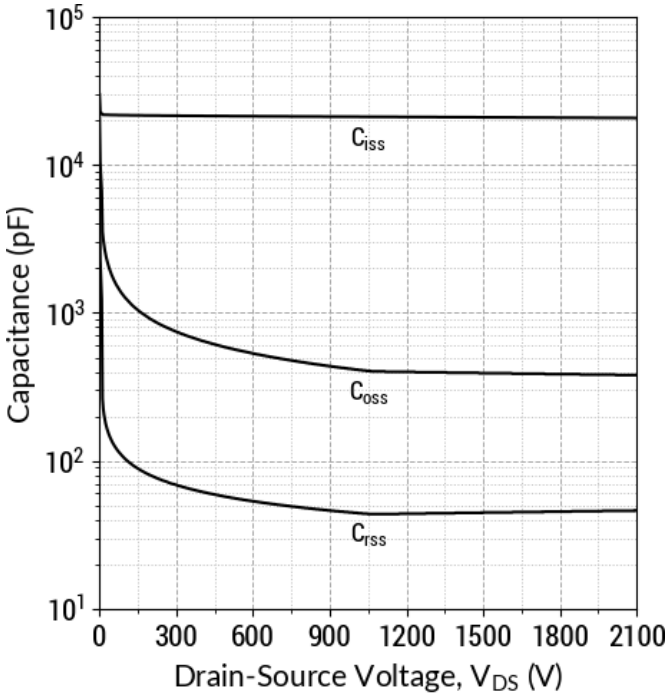
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; I_D = 135 mA

Fig 11: Typical Gate Charge Characteristics



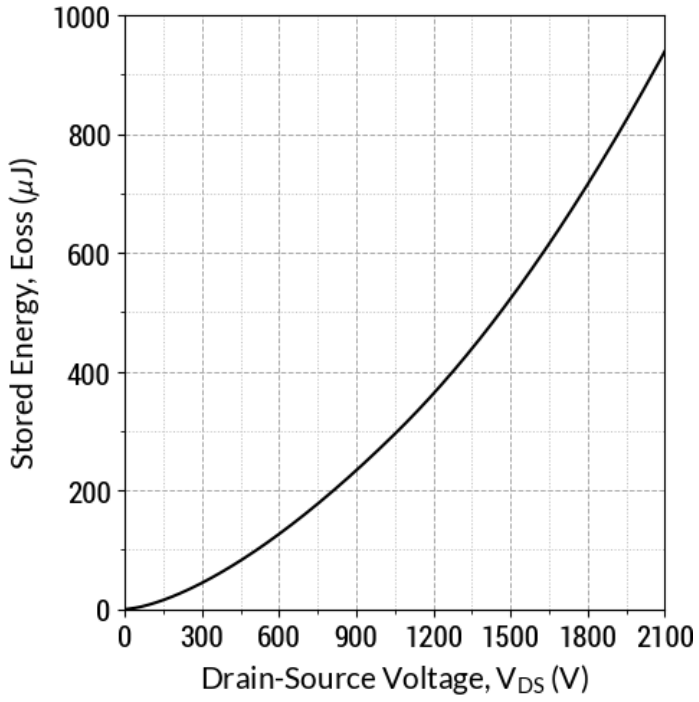
I_D = 135 A; V_{DS} = 1500 V; T_c = 25°C

Fig 12: Typical Capacitance v/s Drain-Source Voltage



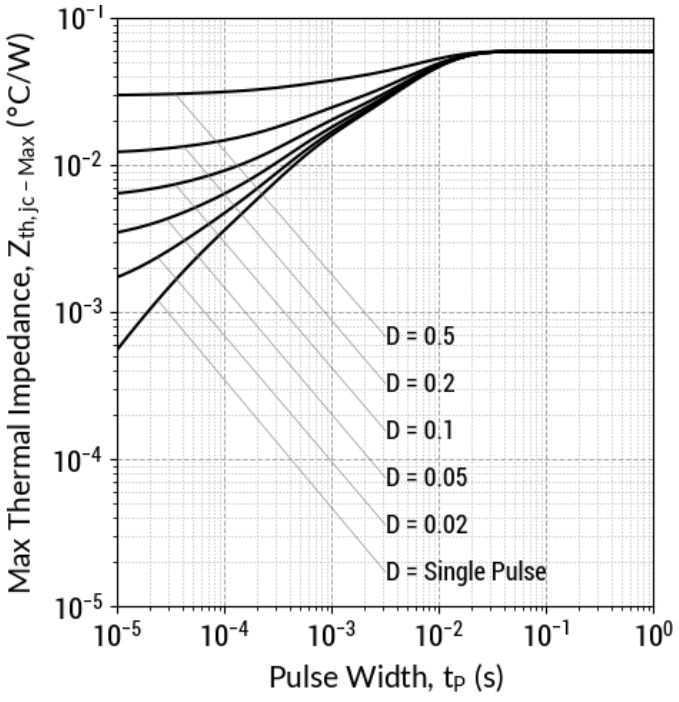
f = 100 KHz; V_{AC} = 25mV

Fig 13: Output Capacitor Stored Energy



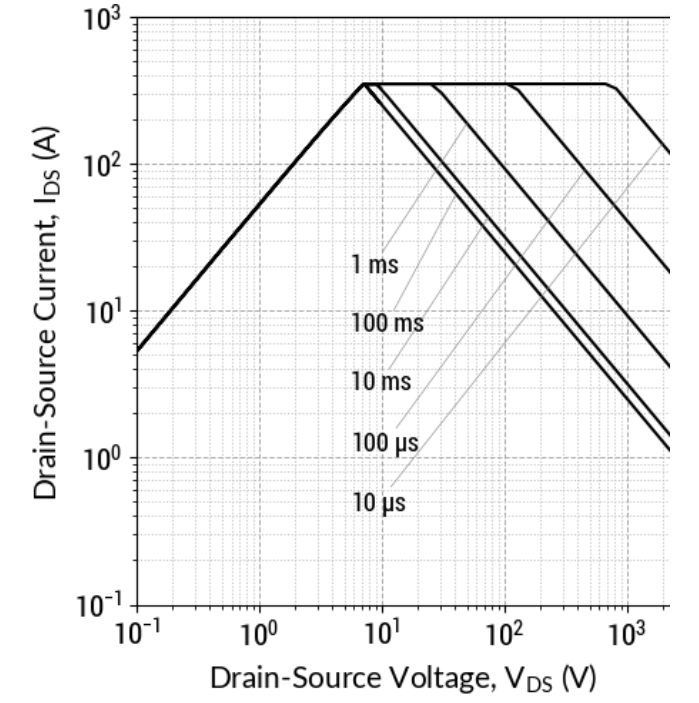
$E_{oss} = f(V_{DS})$

Fig 14: Transient Thermal Impedance



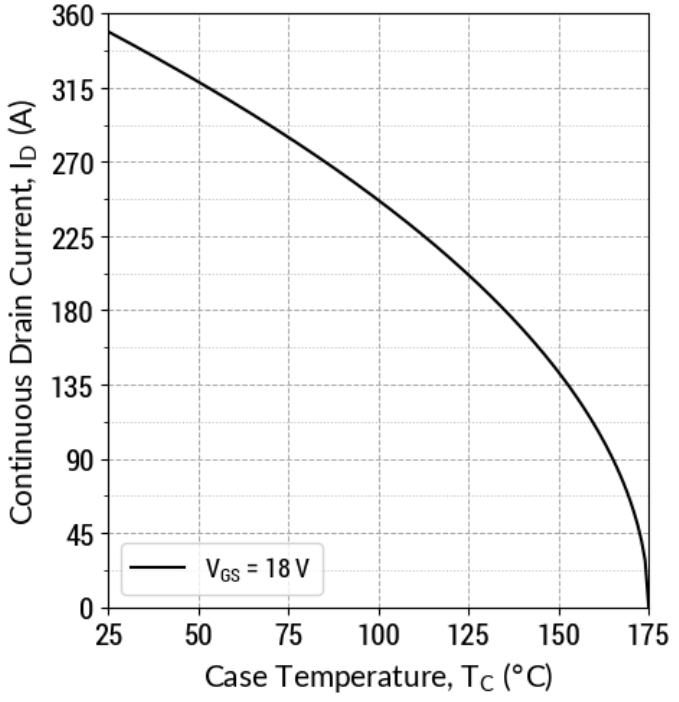
$Z_{th,jc} = f(t_P,D)$; $D = t_P/T$

Fig 15: Safe Operating Area (T_c = 25°C)



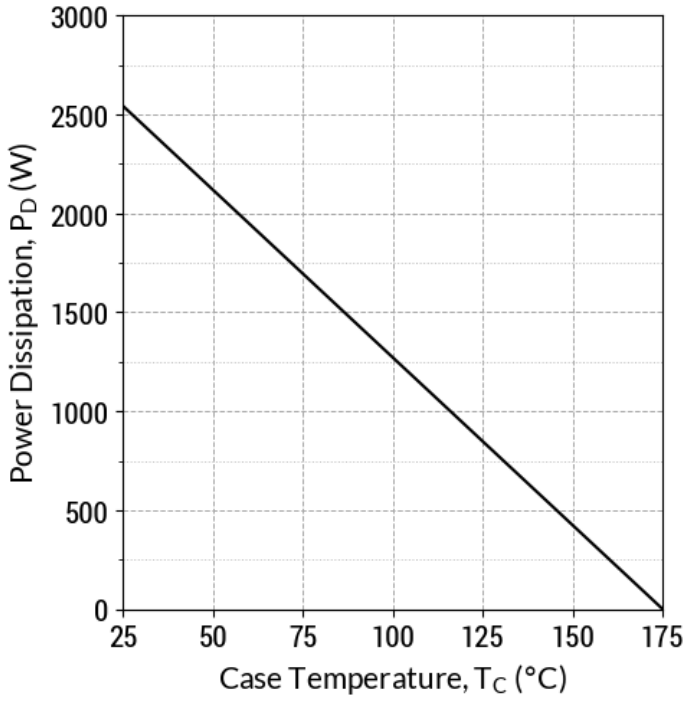
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; $D = 0$

Fig 16: Current De-rating Curve



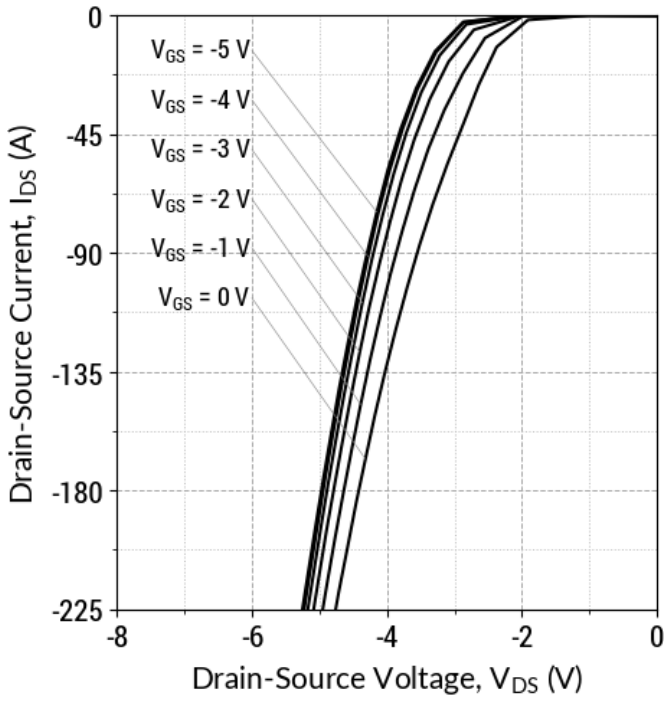
$I_D = f(T_C)$; $T_j \leq 175°C$

Fig 17: Power De-rating Curve



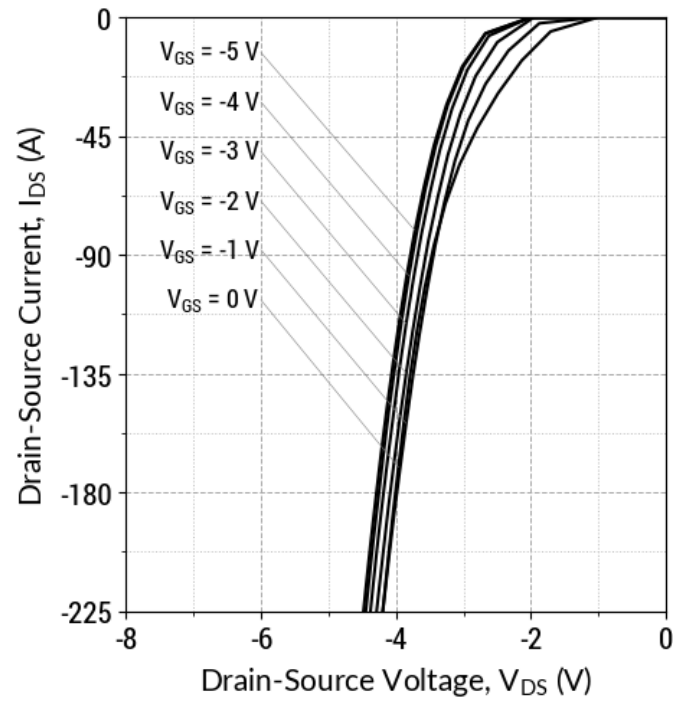
$P_D = f(T_C)$; $T_j \leq 175°C$

Fig 18: Typical Body Diode Characteristics (T_j = 25°C)



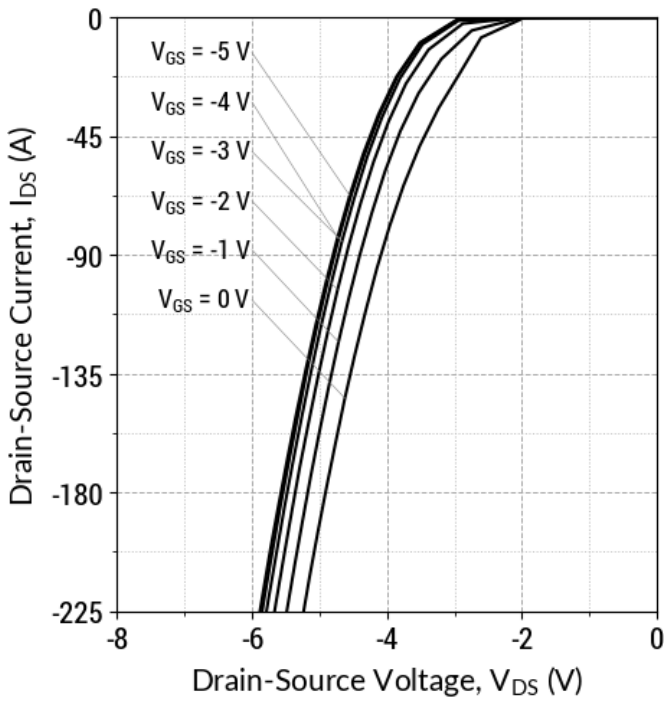
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 19: Typical Body Diode Characteristics (T_j = 175°C)



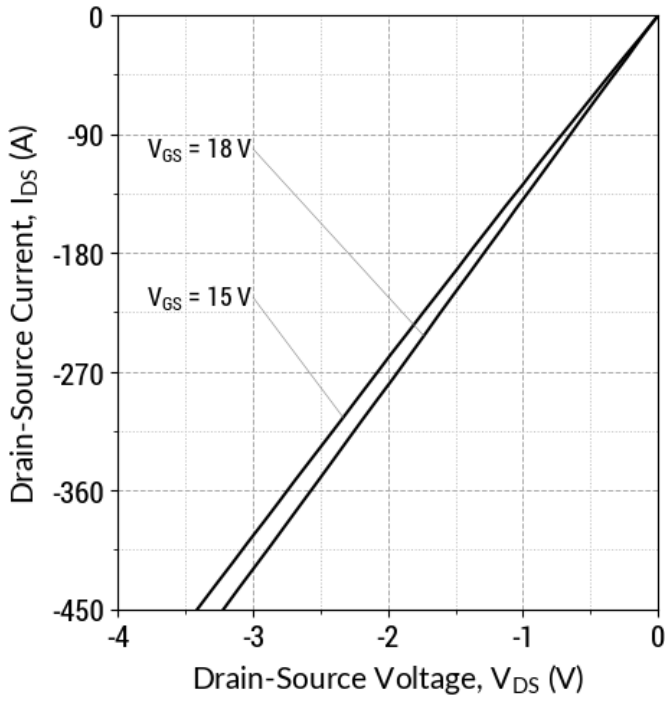
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 20: Typical Body Diode Characteristics (T_j = -55°C)



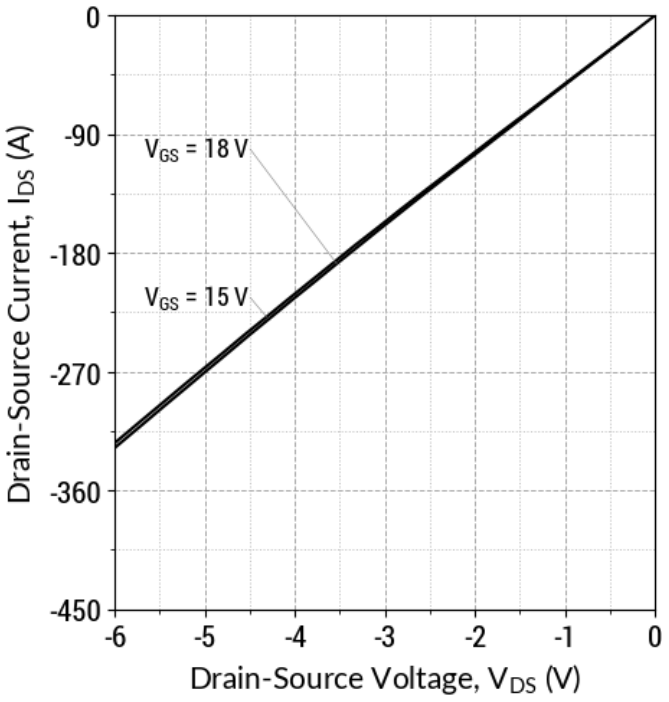
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 21: Typical Third Quadrant Characteristics (T_j = 25°C)



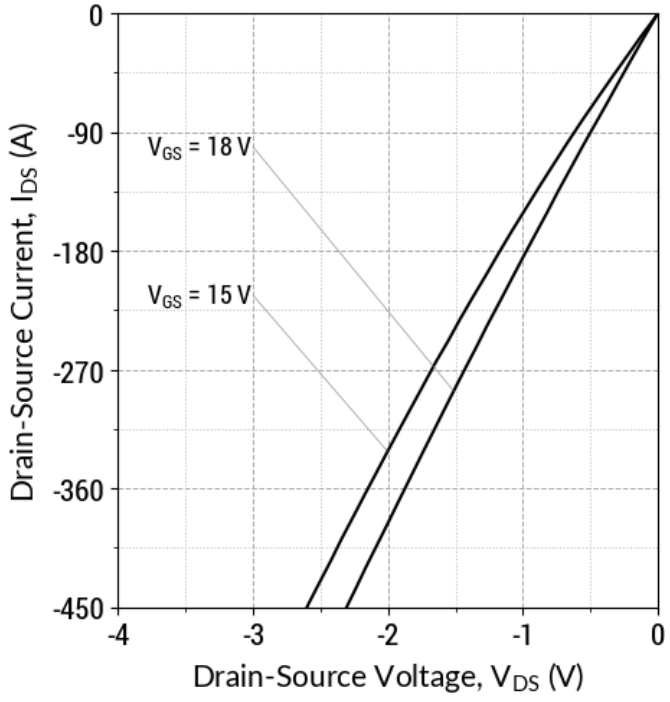
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 22: Typical Third Quadrant Characteristics (T_j = 175°C)



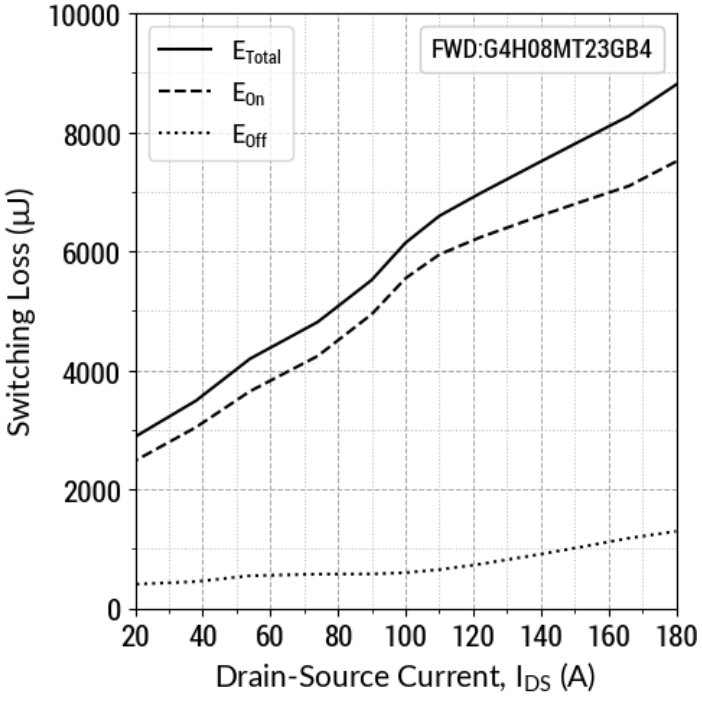
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 23: Typical Third Quadrant Characteristics (T_j = -55°C)



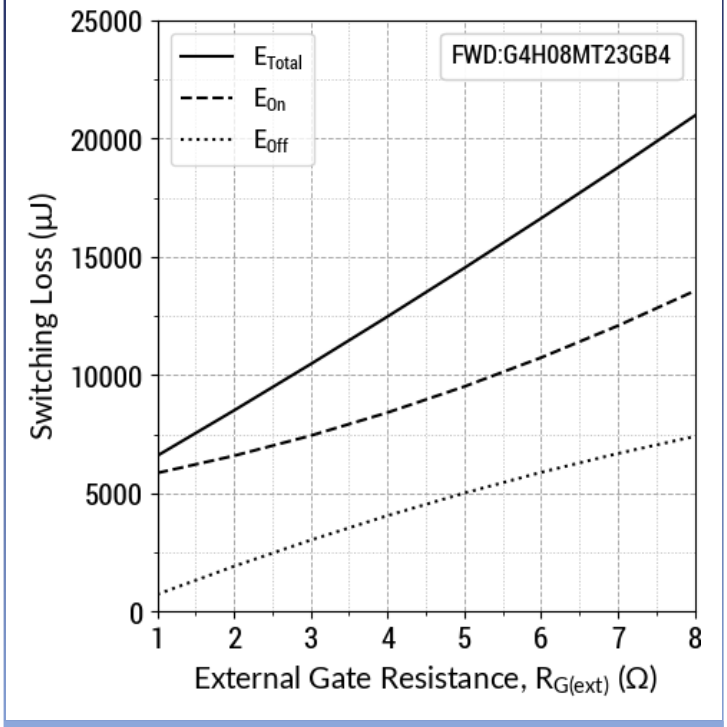
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 24: Inductive Switching Energy v/s Drain Current (V_{DD} = 1500V)



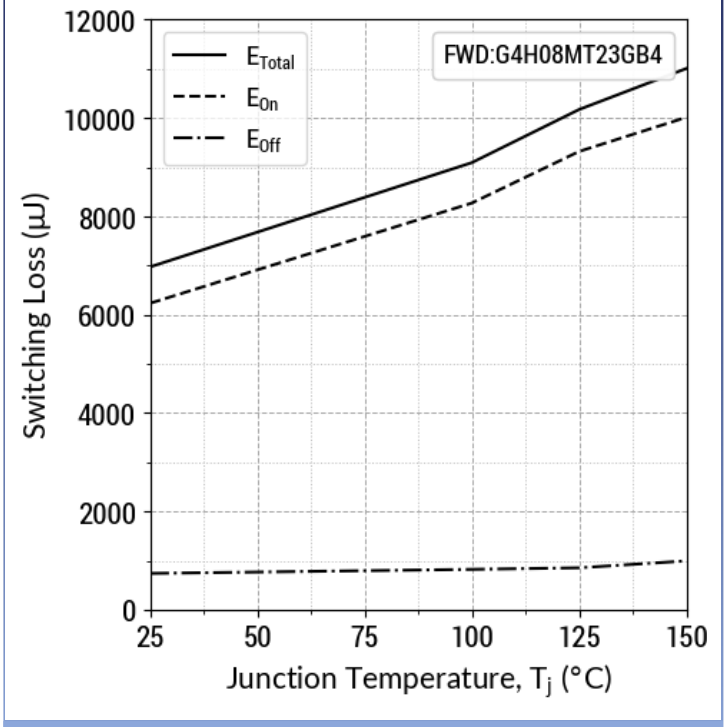
T_j = 25°C; V_{GS} = -5/+18V; $R_{G,on(ext)}$ = 2 Ω; $R_{G,off(ext)}$= 1 Ω

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 1500V)



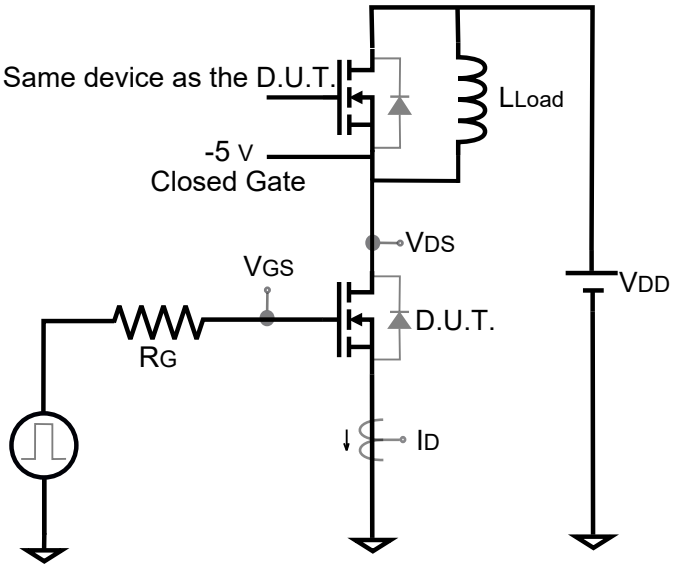
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 120 A

Fig 26: Inductive Switching Energy v/s Temperature (V_{DD} = 1500V)



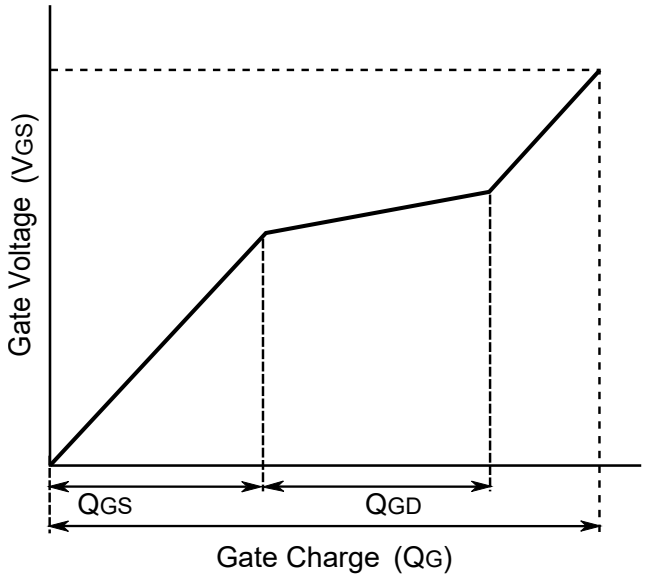
V_{GS} = -5/+18V; $R_{G,on(ext)}$ = 2 Ω; $R_{G,off(ext)}$= 1 Ω; I_{DS} = 120 A

Dynamic Test Circuit

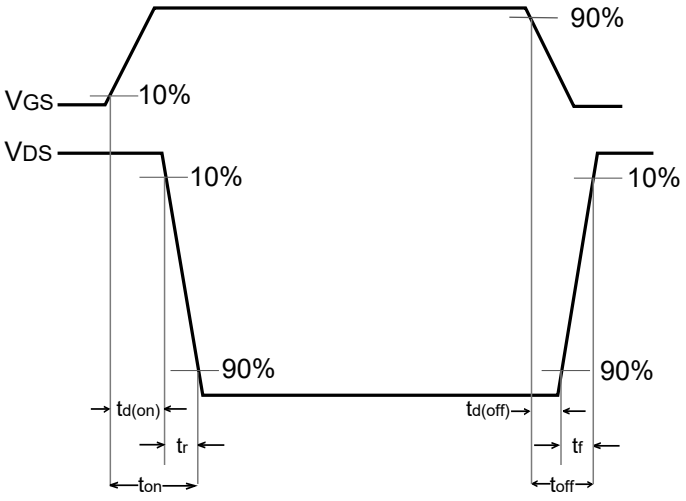


Note: Gate Charge, Switching Time and Energy Circuit

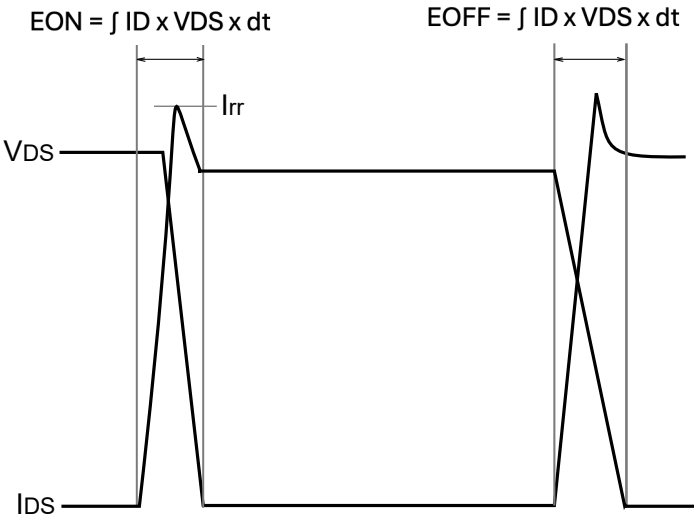
Gate Charge Waveform



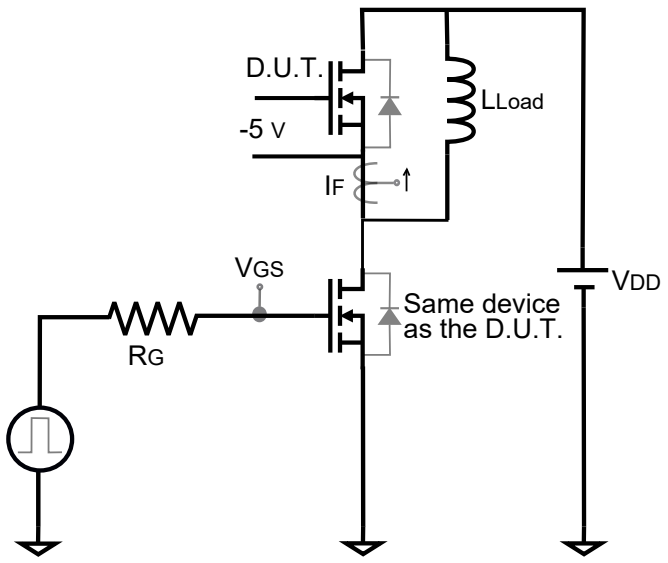
Switching Time Waveform



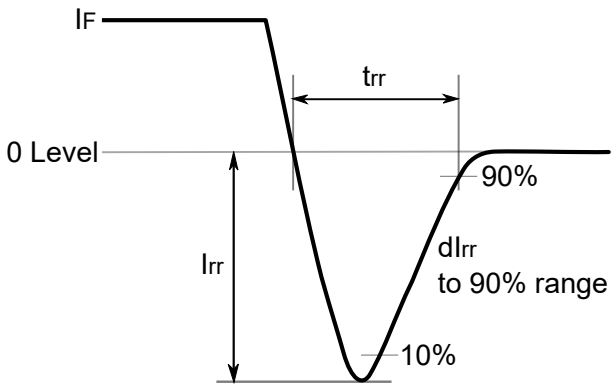
Switching Energy Waveform



Reverse Recovery Circuit

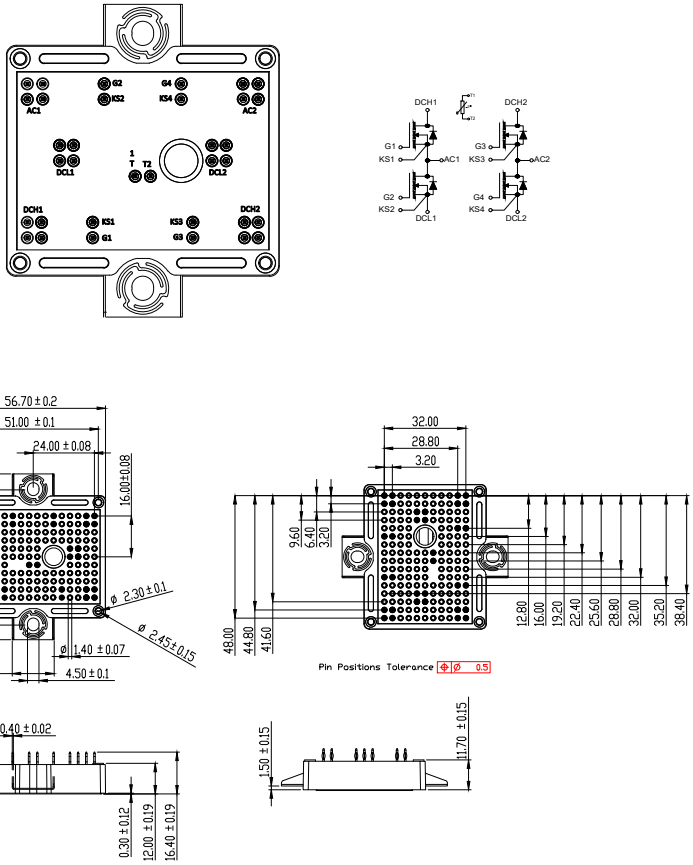


Reverse Recovery Waveform



Package Dimensions

SiCPAK G+ Package Outline



NOTE

1. CONTROLLED DIMENSION IS MILLIMETER.
2. DIMENSIONS DO NOT INCLUDE END FLASH, MOLD FLASH, MATERIAL PROTRUSIONS.

Product Ordering Information

Orderable Part number (OPN)	Package	Packing Method
G4H08MT23GB4HC	SiCPAK G+	Box (Qty = 48)

Product Ordering Information

Orderable Part number (OPN)	Package	Packing Method
G4H08MT23GB4HC-T	SiCPAK G+ With Pre-Applied TIM	Box (Qty = 48)

Revision History

• Rev 26/Aug: Preliminary Specification rev1.2

IMPORTANT NOTICES AND DISCLAIMERS

EXCEPT TO THE EXTENT THAT INFORMATION IN THIS DATA SHEET IS EXPRESSLY AND SPECIFICALLY WARRANTED IN WRITING BY NAVITAS SEMICONDUCTOR ("**NAVITAS**"), EITHER PURSUANT TO THE TERMS AND CONDITIONS OF THE LIMITED WARRANTY CONTAINED IN NAVITAS' STANDARD TERMS AND CONDITIONS OF SALE OR A WRITTEN AGREEMENT SIGNED BY AN AUTHORIZED NAVITAS REPRESENTATIVE, (1) ALL INFORMATION IN THIS DATA SHEET OR OTHER RELIABILITY AND TECHNICAL DATA, AND ANY OTHER DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE OR TOOLS, SAFETY INFORMATION AND OTHER RESOURCES, ARE PROVIDED "AS IS" AND WITH ALL FAULTS; AND (2) NAVITAS MAKES NO WARRANTIES OR REPRESENTATIONS AS TO ANY SUCH INFORMATION OR RESOURCES, IN THIS DATA SHEET OR OTHERWISE, AND HEREBY DISCLAIMS ALL WARRANTIES, EXPRESS AND IMPLIED, INCLUDING WITHOUT LIMITATION ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

CUSTOMER RESPONSIBILITIES. This data sheet and other design resources and information provided by Navitas are intended only for technically trained and skilled developers designing with Navitas- or GeneSiC-branded products ("**Products**"). Performance specifications and the operating parameters of Products described herein are determined in the independent state and may not perform the same way when installed in customer products. The customer (or other user of this data sheet) is solely responsible for (a) designing, validating and testing the products and systems in which Products are incorporated; (b) designing, validating and testing the application in which Products are incorporated; (c) ensuring the application meets applicable standards and any safety, security, regulatory or other requirements; (d) evaluating the suitability of Products for the intended application and the completeness of the information in this data sheet with respect to such application; (e) procuring and/or developing production firmware, if applicable; and (f) completing system qualification, compliance and safety testing, EMC testing, and any automotive, high-reliability or other system qualifications that apply.

UNINTENDED USES OF PRODUCTS. Except to the extent expressly provided in a writing signed by an authorized Navitas representative, Products are not designed, intended or warranted for use in extreme or hazardous conditions; aircraft navigation, communication or control systems; aircraft power and propulsion systems; air traffic control systems; military, weapons, space-based or nuclear applications; life-support devices or systems, including but not limited to devices implanted into the human body and emergency medical equipment; or applications where product failure could lead to death, personal injury or severe property or environmental damage. The customer or other persons using Products in such applications without Navitas' agreement or acknowledgement, as set forth in a writing signed by an authorized Navitas representative, do so entirely at their own risk and agree to fully indemnify Navitas for any damages resulting from such improper use. In order to minimize risks associated with such applications, you should provide adequate design and operating safeguards.

CHANGES TO, AND USE OF, THIS DATA SHEET. This data sheet and accompanying information and resources are subject to change without notice. Navitas grants you permission to use this data sheet and accompanying resources only for the development of an application that uses the Products described herein and subject to the notices and disclaimers set forth above. Any other use, reproduction or display of this data sheet or accompanying resources and information is prohibited. No license is granted to any Navitas intellectual property right or to any third-party intellectual property right. Navitas disclaims any responsibility for, and you will fully indemnify Navitas and its representatives against, any claims, damages, costs, losses and liabilities arising out of your use of this data sheet and any accompanying resources and information.

TERMS AND CONDITIONS. All purchases and sales of Products are subject to Navitas' Standard Terms and Conditions of Sale, including the limited warranty contained therein, unless other terms and conditions have been agreed in a writing signed by an authorized Navitas representative. This data sheet, and Navitas' provision of this data sheet or other information and resources, do not expand or otherwise alter those terms and conditions.

Navitas, GeneSiC, the Navitas and GeneSiC logos, GaNFast, GaNSafe, SICPAK and other Navitas marks used herein are trademarks or registered trademarks of Navitas Semiconductor Limited or its affiliates. Other trademarks used herein are the property of their respective owners.

Copyright © 2026 Navitas Semiconductor Limited and affiliates. All rights reserved.

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.