1200V 18.5mΩ Full-Bridge SiC Module

SiCPAK™ F Series

Trench-Assisted Planar Technology

V_{DS}	=	1200 V
$R_{DS(ON)}$	=	18.5 mΩ
$I_{D,DC}$ (65°C)	=	53 A

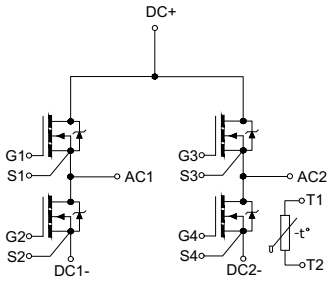
Built for Performance and Endurance

- Epoxy-resin potting and trench-assisted planar SiC MOSFET technology for long-lasting reliability
- Engineered and qualified to withstand harsh stress, temperature variations, and power cycling
- Low on-resistance $R_{DS(ON)}$ across temperature
- Optimized switching speed and balanced Q_{GD}/Q_{GS} for faster, cleaner, and efficient switching performance
- Stable and consistent $V_{GS,th}$ for excellent current sharing and reliable switching
- Outstanding short-circuit & avalanche (UIS) performance
- THB (HV-H3TRB) qualification at module-level & die-level
- Optional pre-applied Thermal Interface Material (TIM), "-T" orderable part number suffix

Package



SiCPAK™ F



Applications

- EV Road Side Chargers
- Solar Inverters
- Energy Storage Systems (ESS)
- Uninterrupted Power Supplies (UPS)
- Motor Control and Drives
- Smard Grid and Distributed Generation
- Induction Heating and Welding

Absolute Maximum (per Switch Position) (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values	Unit	Note
Drain-Source Voltage	$V_{DS,max}$	V_{GS} = 0 V, I_D = 100 µA	1200	V	
Gate-Source Voltage (Dynamic)	$V_{GS,max}$	Transient	-10/+22	V	
Gate-Source Voltage (Operation)	$V_{GS,op}$	Static	-5/+18	V	Note 1
Virtual Junction Temperature	T_j	Operation	-40 to 175	°C	
Power Dissipation	P_D	T_H = 65°C, $T_{j,op}$ ≤ 175°C T_H = 120°C, $T_{j,op}$ ≤ 175°C	106 53	W	Fig. 17
DC Continuous Drain Current	$I_{D,DC}$	T_H = 65°C, $T_{j,op}$ ≤ 175°C, V_{GS} = 18 V T_H = 120°C, $T_{j,op}$ ≤ 175°C, V_{GS} = 18 V	53 37	A	Fig. 16

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

Note 1: Recommended operating (static) on-state gate voltage is +15V to +18V and off-state gate voltage is -5V to -3V

SEE IMPORTANT NOTICES AND DISCLAIMERS AT THE END OF THIS DATA SHEET REGARDING THE INFORMATION IN THIS DATA SHEET, THE USE OF OUR PRODUCTS, AND YOUR RESPONSIBILITIES RELATING TO SUCH USE.

Electrical Characteristics (per Switch Position) (At T_C = 25°C Unless Otherwise Stated)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Drain-Source Breakdown Voltage	V_{DSS}	V_{GS} = 0 V, I_D = 100 µA	1200			V	
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 1200 V, V_{GS} = 0 V		1		µA	
Gate Source Leakage Current	I_{GSS}	V_{GS} = 22V, V_{DS} = 0V V_{GS} = -10V, V_{DS} = 0V			100 -100	nA	
Gate Threshold Voltage	$V_{GS,th}$	V_{DS} = V_{GS}, I_D = 35 mA V_{DS} = V_{GS}, I_D = 35 mA, T_j = 175°C	2.2	2.7 2.0	4.3	V	Note 2
Drain-Source On-State Resistance	$R_{DS(ON)}$	V_{GS} = 18V, I_D = 45 A V_{GS} = 18V, I_D = 45 A, T_j = 175°C		18.5 31.5	24.0	mΩ	Note 3,4 Fig. 6-9
Input Capacitance	C_{iss}	V_{DS} = 800V, V_{GS} = 0V f = 100kHz, V_{AC} = 25mV		4925		pF	Fig. 12
Output Capacitance	C_{oss}			182			
Reverse Transfer Capacitance	C_{rss}			11			
Internal Gate Resistance	$R_{G,int}$	V_{GS} = 18V, f = 500kHz, V_{AC} = 25mV		1.3		Ω	
Gate-Source Charge	Q_{GS}	V_{DS} = 800V, V_{GS} = +18/-5V I_D = 45 A Per JEDEC JEP-192		56		nC	Fig. 11
Gate-Drain Charge	Q_{GD}			39			
Total Gate Charge	Q_G			196			
Turn-On Switching Energy (Body Diode)	E_{On}	T_j = 25°C, V_{GS} = -5/+18V, $R_{G(ext)}$ = 6 Ω, L = 60 µH, I_D = 80 A, V_{DD} = 800 V		1759		µJ	Fig. 24-27
Turn-Off Switching Energy (Body Diode)	E_{Off}			114			
Rise Time	t_r	V_{DD} = 800 V, V_{GS} = -5/+18V $R_{G(ext)}$ = 6 Ω, L = 60 µH, I_D = 80 A Timing relative to V_{DS}, Inductive load		16		ns	Fig. 26
Fall Time	t_f			26			

Body Diode Characteristics (per Switch Position) (At T_j = 25°C unless otherwise specified)

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Diode Forward Voltage	V_{SD}	V_{GS} = -5V, I_{SD} = 22 A V_{GS} = -5V, I_{SD} = 22 A, T_j = 175°C		4.5 4.1		V	Fig. 18,19
DC Continuous Diode Current	I_{SD}	T_H = 65 °C, $T_{j,op}$ ≤ 175 °C, V_{GS} = -5 V T_H = 120 °C, $T_{j,op}$ ≤ 175 °C, V_{GS} = -5 V		33 20		A	

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

Note 2: Tested after applying +25V for 80ms
Note 3: Device(Die) ON State resistance only: Package resistance reported separately in module characteristics
Note 4: Total effective resistance per switch postition (HS or LS) = MOSFET $R_{DS(ON)}$ + package resistance by switch position

Module Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Thermal Resistance, Junction - Heatsink	R_{thJHS}	per switch TIM = 80 µm , λ = 4.4 W/(m.K)		0.94		°C/W	Fig. 14
Case Temperature	T_C		-40		150	°C	
Stray Inductance	L_{stray}	Between DC+ and DC- f = 10 MHz		8.63		nH	
Package Resistance, HS	R_{HS}	T_C = 125 °C		1.66		mΩ	Note 4
Package Resistance, LS	R_{LS}	T_C = 125 °C		1.7			
Weight	W			28.1		g	
Case Isolation Voltage	V_{iso}	AC 50 Hz, 60s		4000		V	
Comparative Tracking Index	CTI	Epoxy-resin EMC		200			
Creepage Distance		Terminal to Terminal Terminal to Heatsink		9.05 12.7		mm	

NTC-Thermistor Characteristics

Parameter	Symbol	Conditions	Values			Unit	Note
			Min.	Typ.	Max.		
Rated Resistance	$R_{NTC,25}$	T_{NTC} = 25 °C		5		kΩ	
Resistance Tolerance	ΔR/R	T_{NTC} = 25 °C	-5		+5	%	
Power Dissipation	$P_{NTC,25}$	T_{NTC} = 25 °C			20	mW	
Beta Value (B-value)	B_{25}/B_{50}	T_2 = 50 °C		3375		K	
	B_{25}/B_{80}	T_2 = 80 °C		3410			
	B_{25}/B_{100}	T_2 = 100 °C		3435			

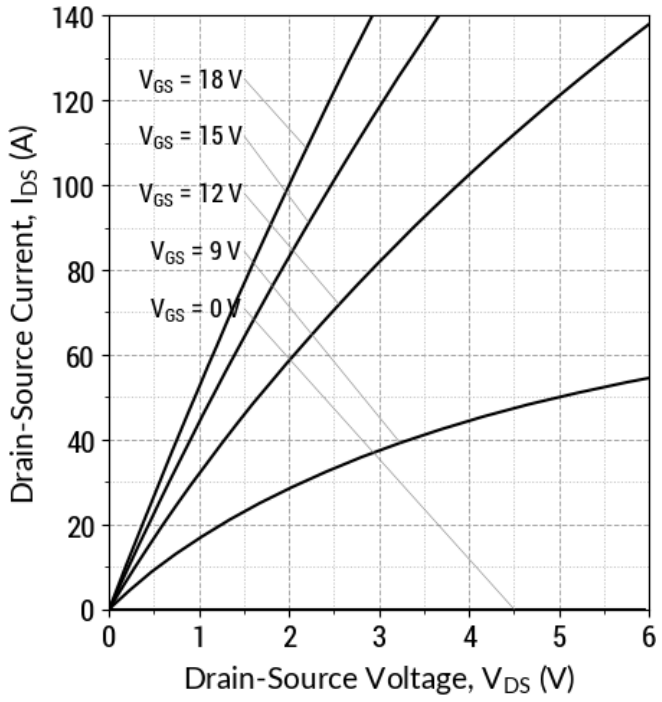
Product Ordering Information

Orderable Part number (OPN)	Package	Packing Method
G3F18MT12FB4	SiCPAK™ F	Box (Qty - 12)
G3F18MT12FB4-T	SiCPAK™ F with TIM	Box (Qty - 12)

NOTE: This datasheet provides preliminary specifications. Parameters, conditions and values are subject to change.

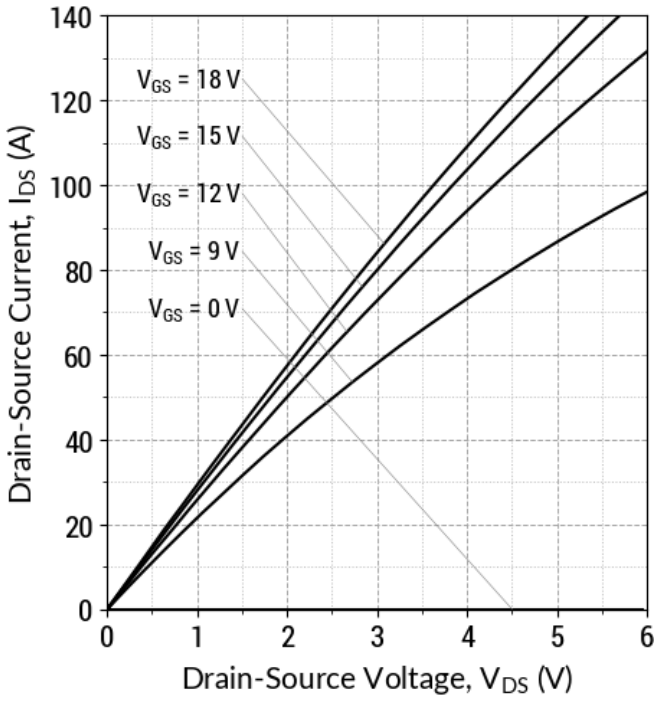
Note 4: Total effective resistance per switch postition (HS or LS) = MOSFET $R_{DS(ON)}$ + package resistance by switch position

Fig 1: Typical Output Characteristics (T_j = 25°C)



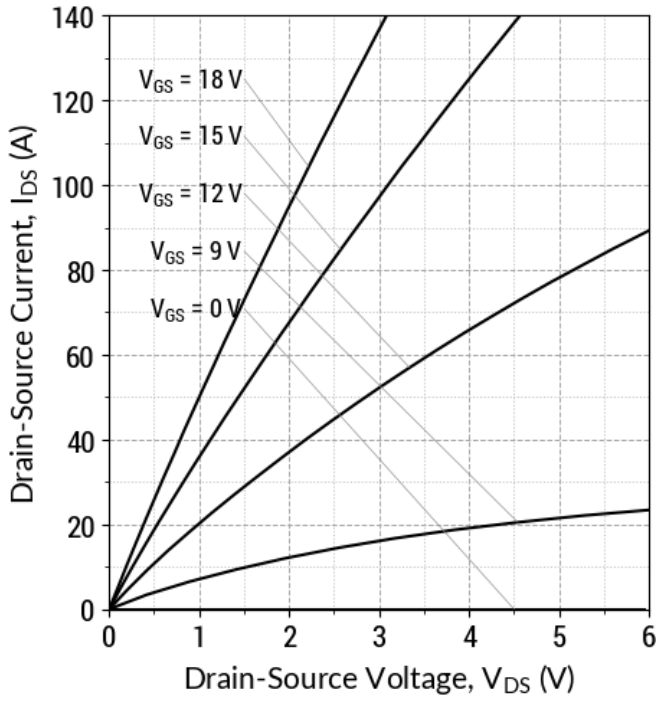
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 2: Typical Output Characteristics (T_j = 175°C)



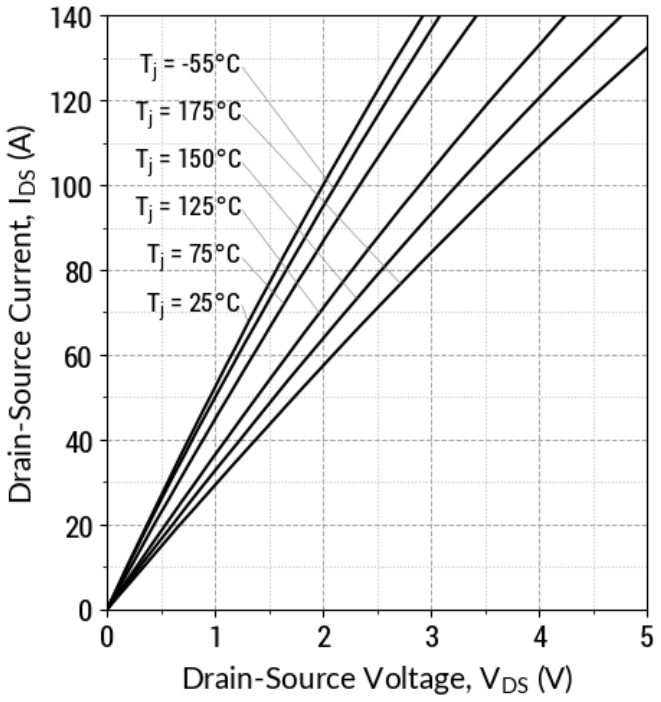
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 3: Typical Output Characteristics (T_j = -55°C)



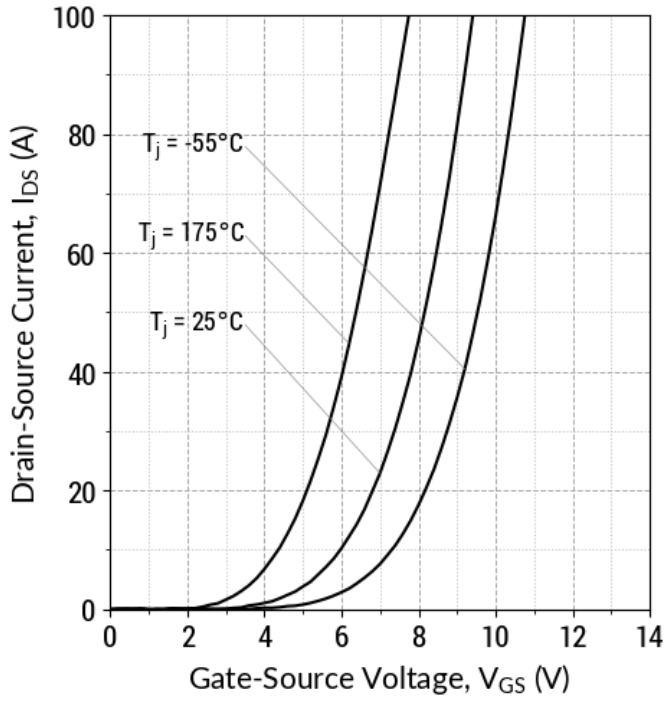
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 4: Typical Output Characteristics (V_{GS} = 18 V)



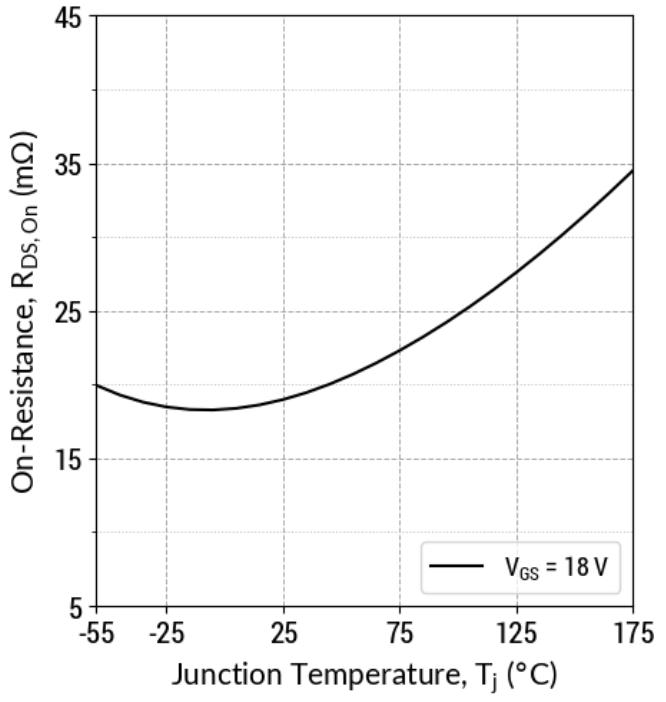
$I_D = f(V_{DS}, T_j)$; t_P = 50 µs

Fig 5: Typical Transfer Characteristics (V_{DS} = 10 V)



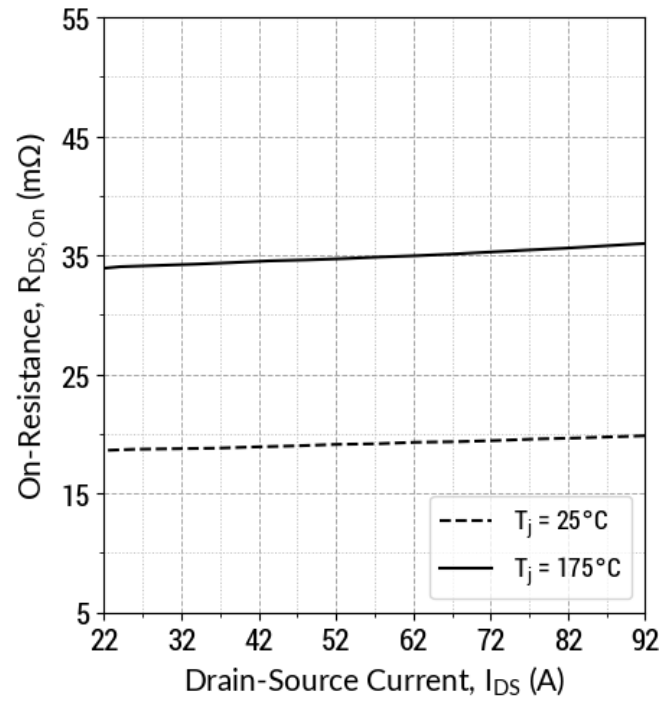
$I_D = f(V_{GS}, T_j)$; t_P = 100 µs

Fig 6: Typical $R_{DS(ON)}$ v/s Temperature



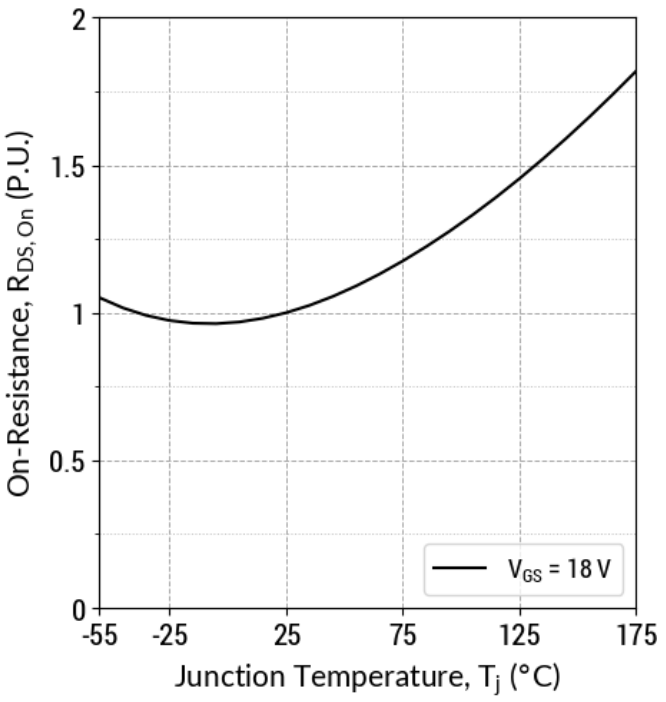
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 45 A

Fig 7: Typical $R_{DS(ON)}$ v/s Drain Current



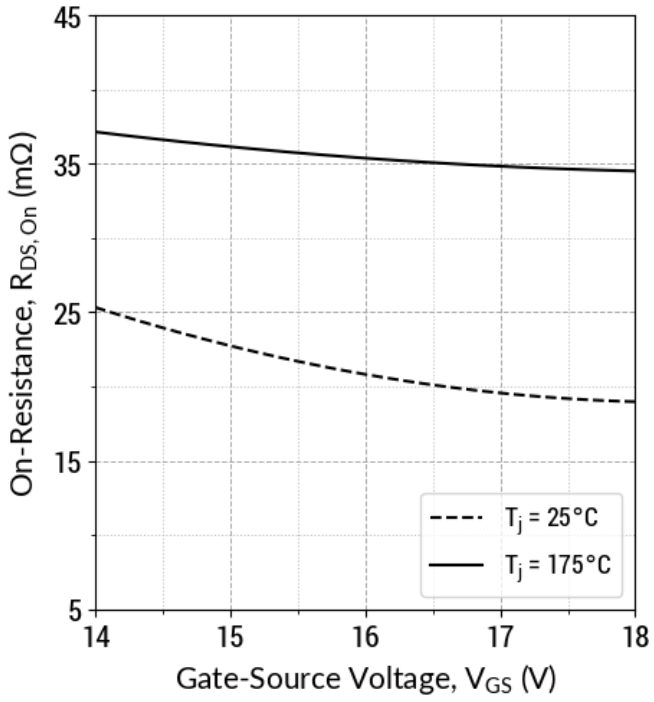
$R_{DS(ON)} = f(T_j, I_D)$; t_P = 50 µs; V_{GS} = 18 V

Fig 8: Typical Normalized $R_{DS(ON)}$ v/s Temperature



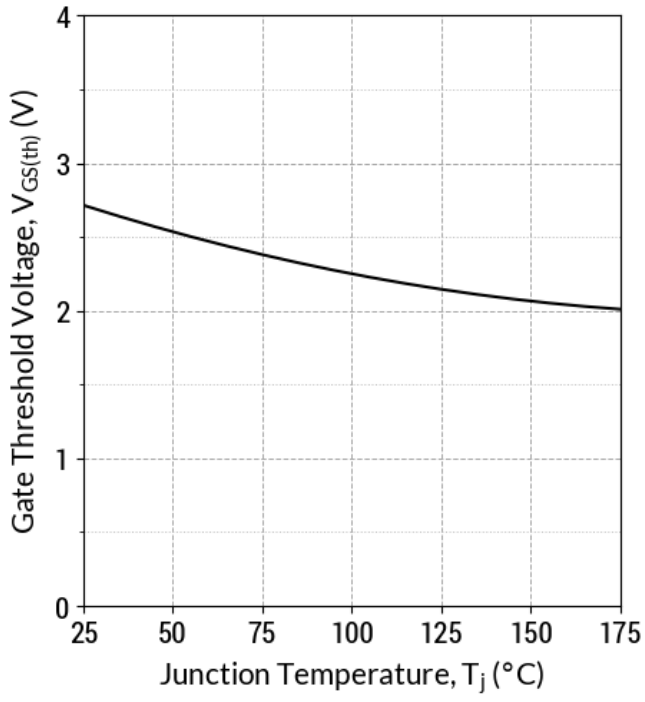
$R_{DS(ON)} = f(T_j)$; t_P = 50 µs; I_D = 45 A

Fig 9: Typical $R_{DS(ON)}$ v/s Gate Voltage



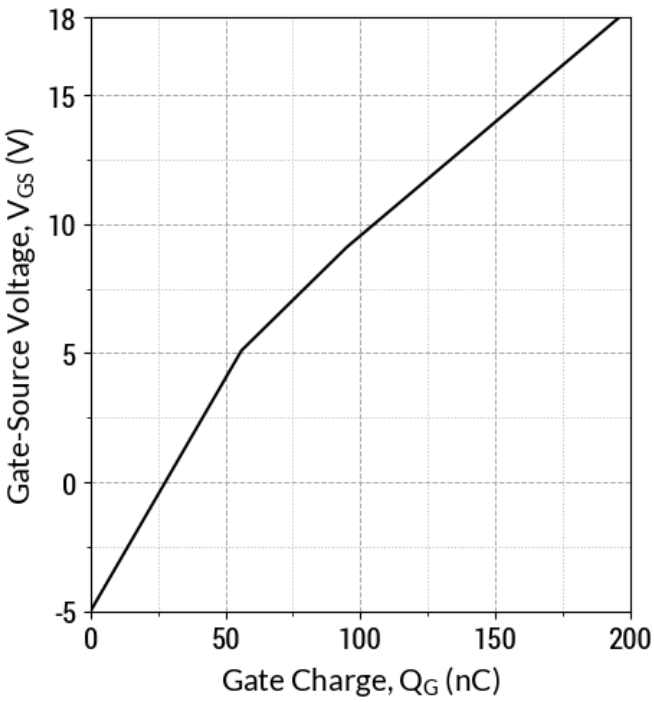
$R_{DS(ON)} = f(T_j, V_{GS})$; t_P = 50 µs; I_D = 45 A

Fig 10: Typical Threshold Voltage Characteristics



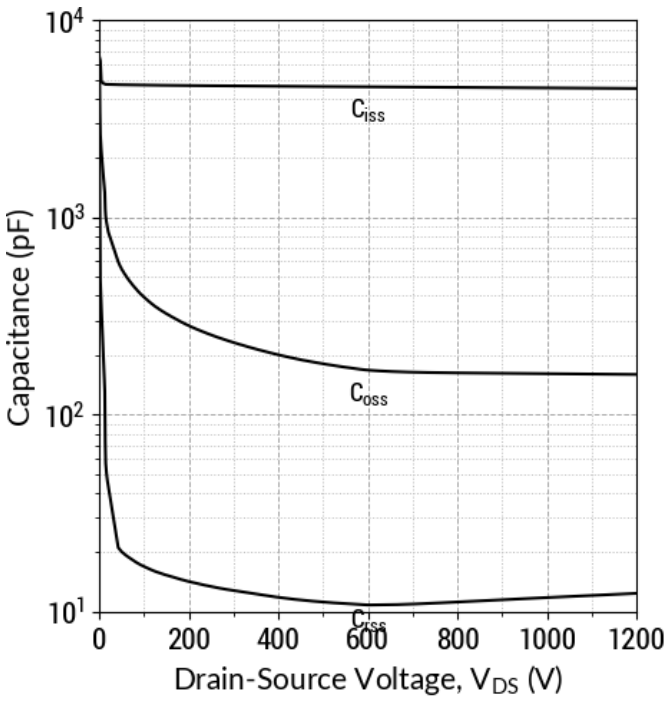
$V_{GS(th)} = f(T_j)$; $V_{DS} = V_{GS}$; I_D = 35 mA

Fig 11: Typical Gate Charge Characteristics



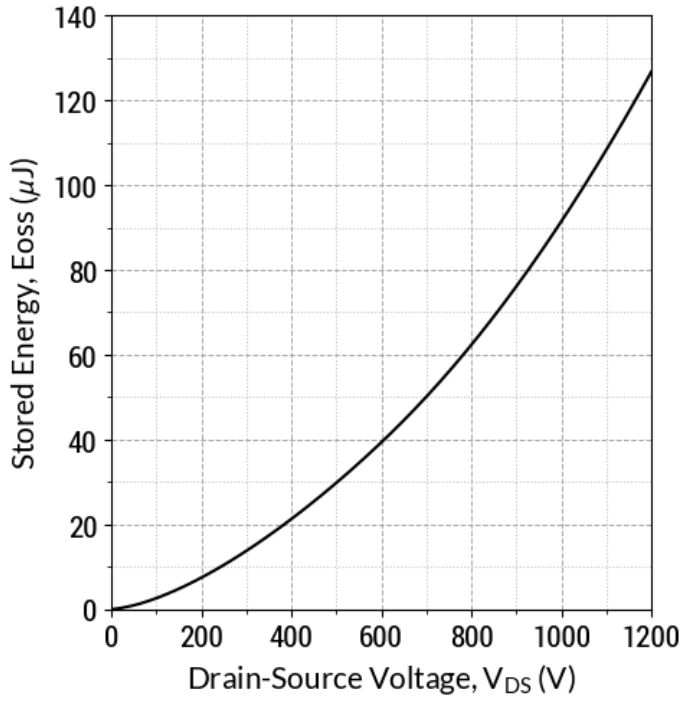
I_D = 45 A; V_{DS} = 800 V; T_c = 25°C

Fig 12: Typical Capacitance v/s Drain-Source Voltage



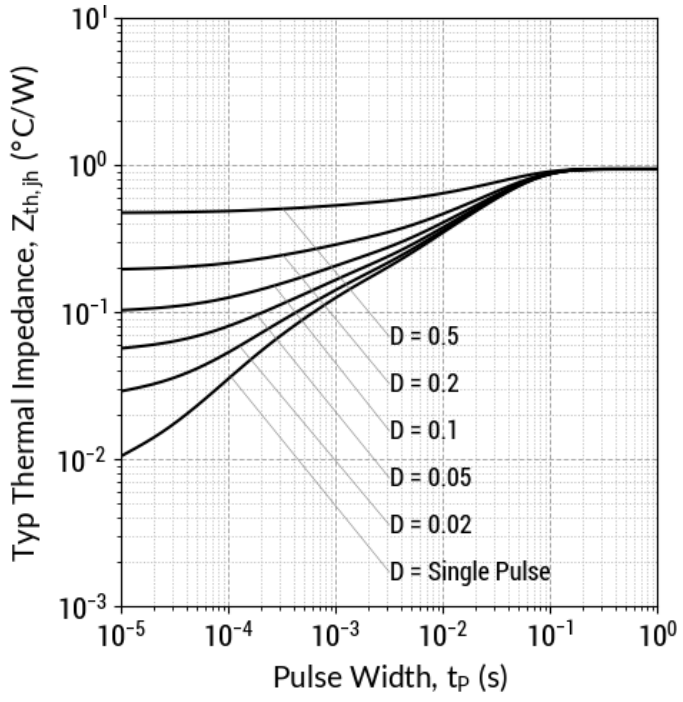
f = 500 KHz; V_{AC} = 25mV

Fig 13: Output Capacitor Stored Energy



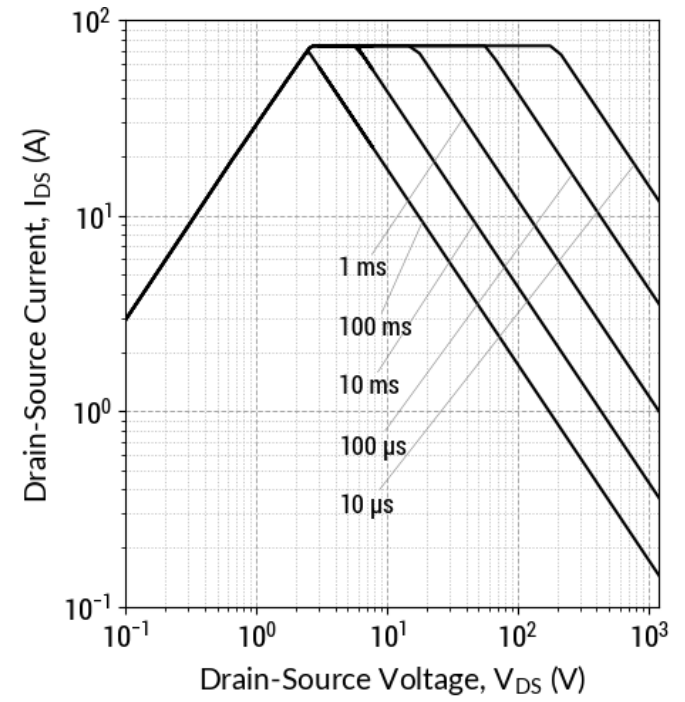
$E_{oss} = f(V_{DS})$

Fig 14: Typical Transient Thermal Impedance



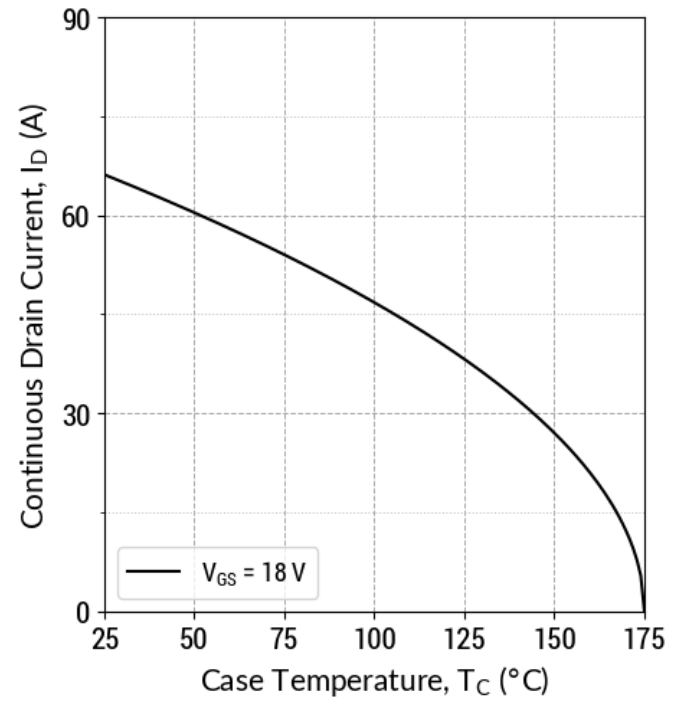
$Z_{th,jh} = f(t_P,D)$; $D = t_P/T$

Fig 15: Safe Operating Area (T_c = 25°C)



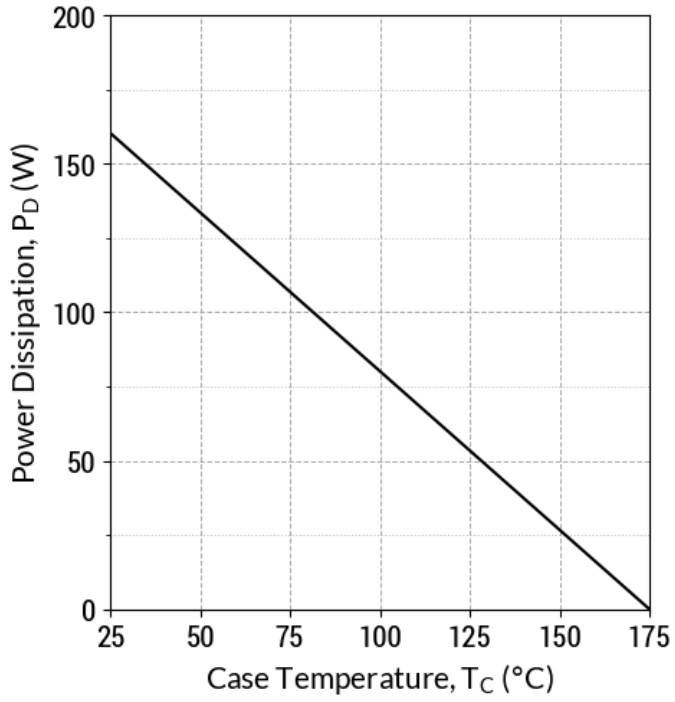
$I_D = f(V_{DS}, t_P)$; $T_j \leq 175°C$; $D = 0$

Fig 16: Current De-rating Curve



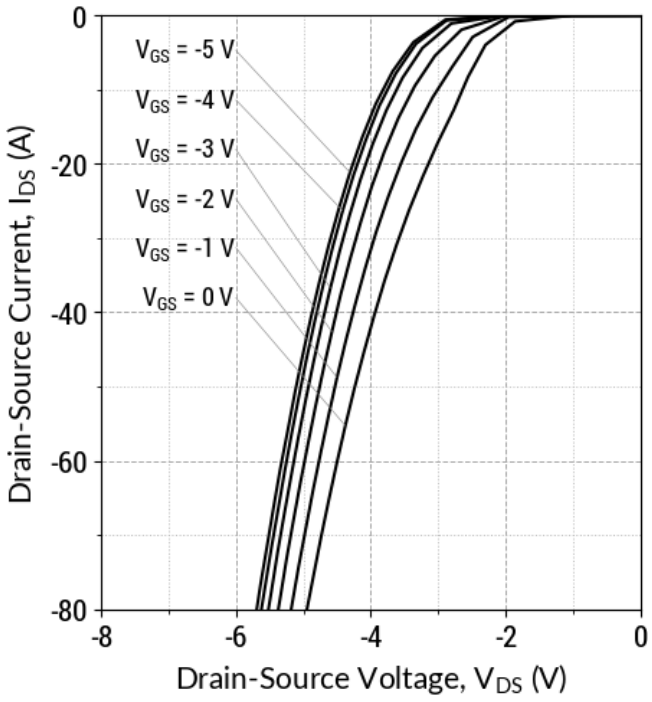
$I_D = f(T_C)$; $T_j \leq 175°C$

Fig 17: Power De-rating Curve



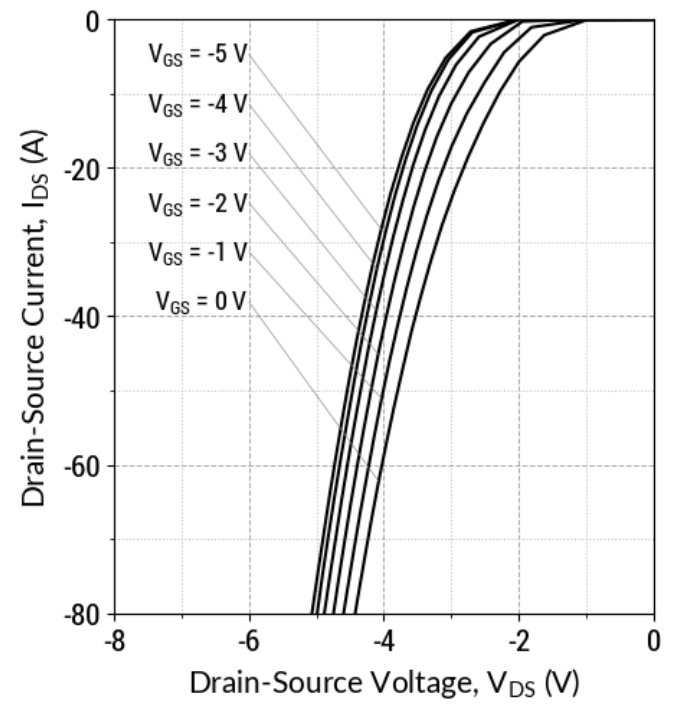
$P_D = f(T_C)$; $T_j \leq 175°C$

Fig 18: Typical Body Diode Characteristics (T_j = 25°C)



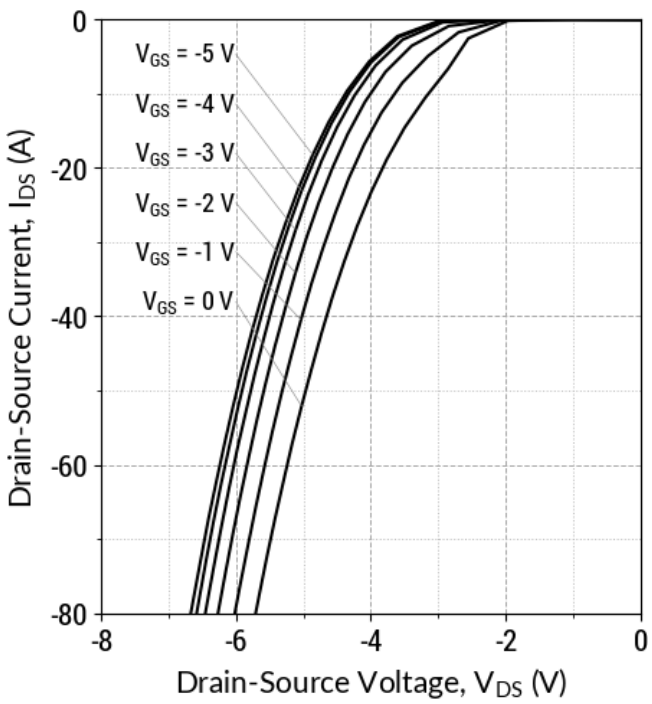
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 19: Typical Body Diode Characteristics (T_j = 175°C)



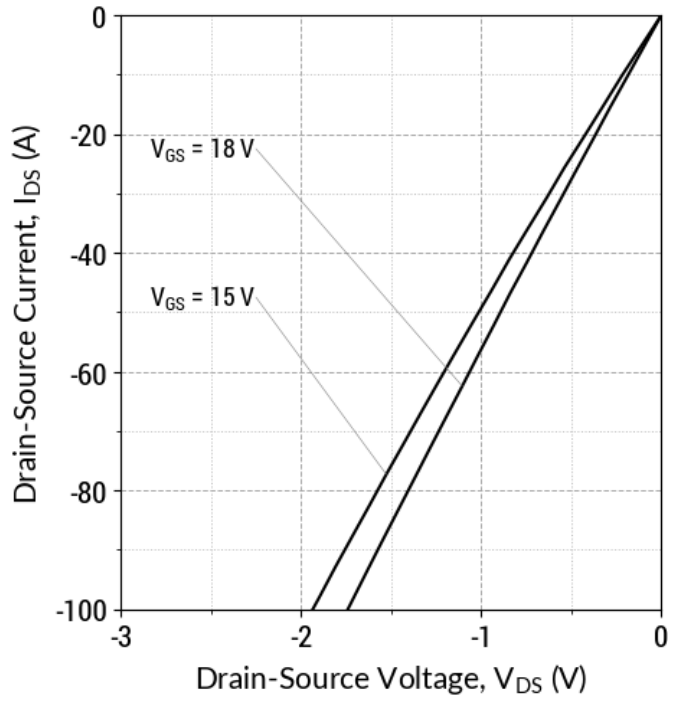
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 20: Typical Body Diode Characteristics (T_j = -55°C)



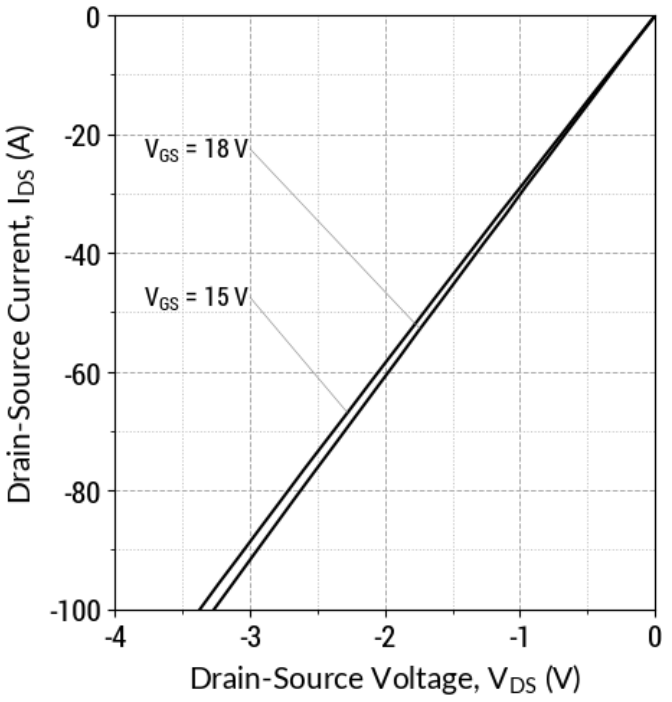
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 21: Typical Third Quadrant Characteristics (T_j = 25°C)



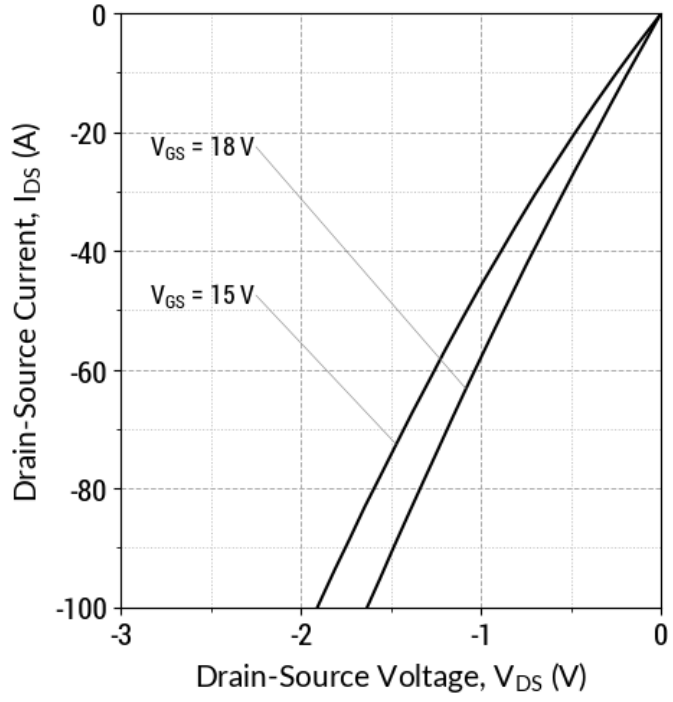
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 22: Typical Third Quadrant Characteristics (T_j = 175°C)



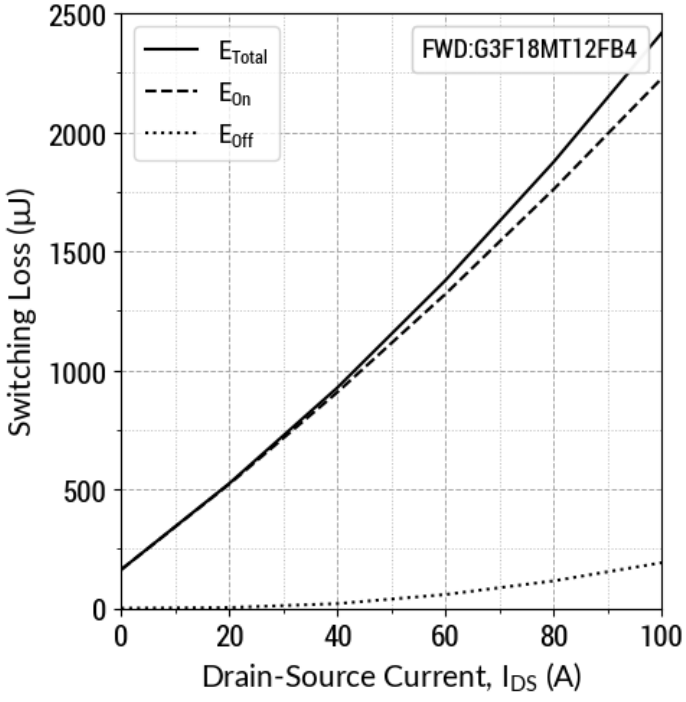
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 23: Typical Third Quadrant Characteristics (T_j = -55°C)



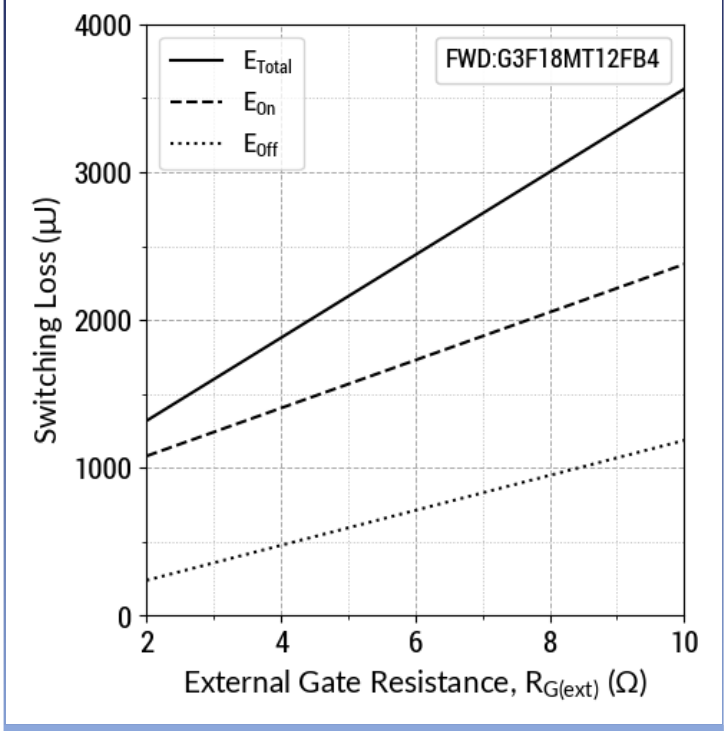
$I_D = f(V_{DS}, V_{GS})$; t_P = 50 µs

Fig 24: Inductive Switching Energy v/s Drain Current (V_{DD} = 800V)



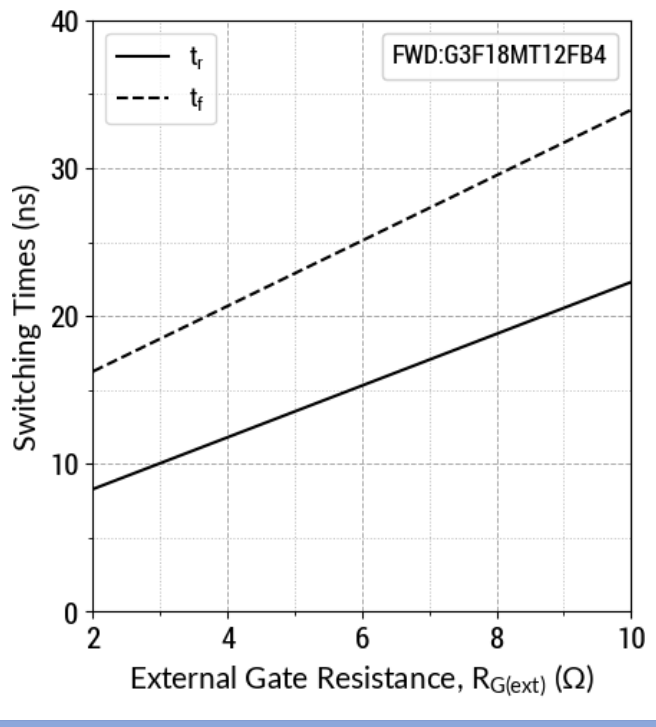
T_j = 25°C; V_{GS} = -5/+18V; $R_{G(on)}$ = 6 Ω; $R_{G(off)}$ = 1 Ω; L = 60µH

Fig 25: Inductive Switching Energy v/s $R_{G(ext)}$ (V_{DD} = 800V)



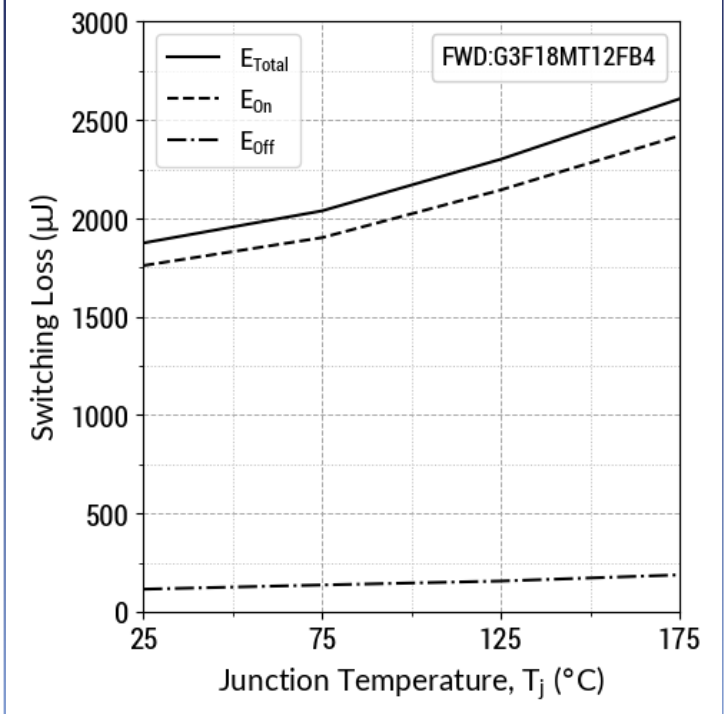
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 80 A; L = 60µH

Fig 26: Switching Time v/s $R_{G(ext)}$ (V_{DD} = 800V)



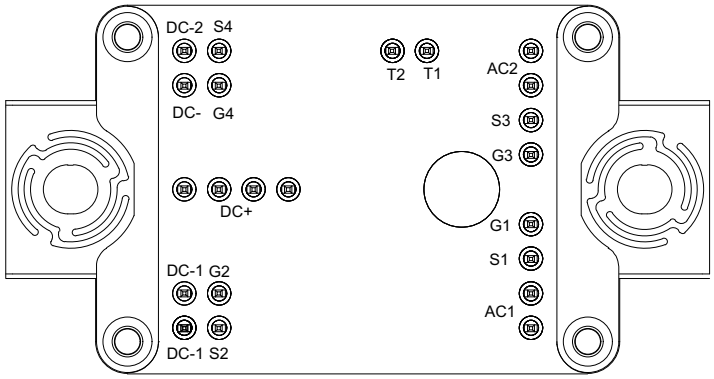
T_j = 25°C; V_{GS} = -5/+18V; I_{DS} = 80 A; L = 60µH

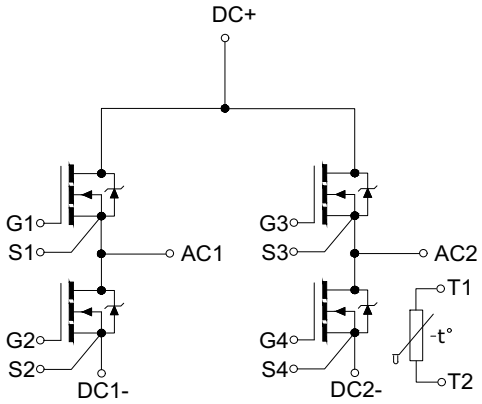
Fig 27: Inductive Switching Energy v/s Temperature (V_{DD} = 800V)



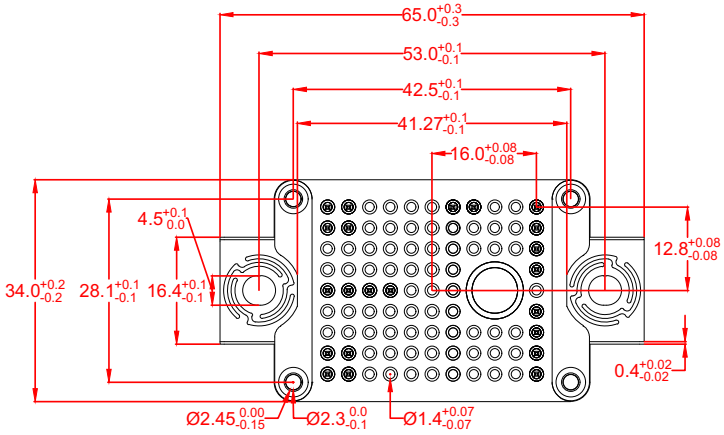
V_{GS} = -5/+18V; $R_{G(on)}$ = 6 Ω; $R_{G(off)}$ = 1 Ω; I_{DS} = 80 A; L = 60µH

Pinout and Package Dimensions

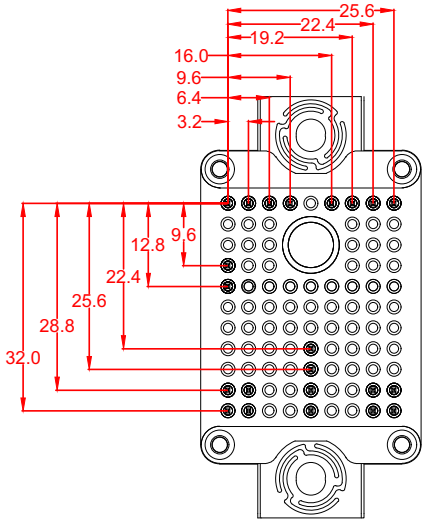




TOP VIEW

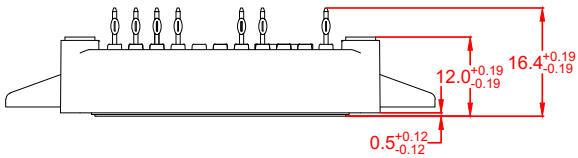


TOP VIEW

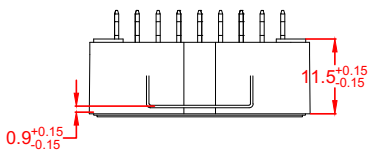


Pin Positions Tolerance ⌖ | Ø 0.5

SIDE VIEW



SIDE VIEW



NOTES

1. Controlled dimension is millimeter (mm)
2. Dimensions do not include material protrusions

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