



APPLICATION NOTE | AN041

Getting Started with the Navitas UHV SiC Double-Pulse Test Board

Reference kit EVB-UHVSIC-GB-E-DPT-1 for 2.3 kV and 3.3 kV SiCPAK™ G+ modules

Document information	
Product	UHV SiCPAK™ G+ Double-Pulse Test Evaluation Board
Reference kit (OPN)	EVB-UHVSIC-GB-E-DPT-1
Board revision	V1
Supported modules	All Navitas UHV SiCPAK™ G+ 2.3 kV and 3.3 kV modules (see Table 1)
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1. Abstract

Characterizing 2.3 kV and 3.3 kV SiC MOSFET modules needs a test fixture with a very small power loop, clean high-voltage measurement points and robust protection. This application note describes the Navitas UHV SiCPAK™ G+ double-pulse test (DPT) evaluation board, EVB-UHVSIC-GB-E-DPT-1: its architecture, specifications, hardware, test setup, operating procedure and the method used to extract switching energies (E_{on} , E_{off} , E_{rr}), switching times and dv/dt , di/dt . The same board supports both voltage classes, and lets any of the four module switches be tested without rework.

2. Introduction

Solid-state transformers for AI data centres, utility-scale battery storage, renewables and medium-voltage drives are moving to ultra-high-voltage (UHV) SiC. Navitas GeneSiC™ 2300 V and 3300 V MOSFETs, built on fourth-generation Trench-Assisted Planar™ (TAP) technology, are offered in SiCPAK™ G+ half-bridge and full-bridge modules. Designers need reliable switching data at the real bus voltage and temperature to size gate drivers, snubbers and cooling.

The board places a film-capacitor DC link, a low-inductance laminated power loop and two plug-in isolated gate-driver cards around a single SiCPAK™ G+ dual half-bridge module. The module mounts on the bottom side against a heatsink or heater plate; the capacitor bank and driver cards sit on the top side (Fig. 1).

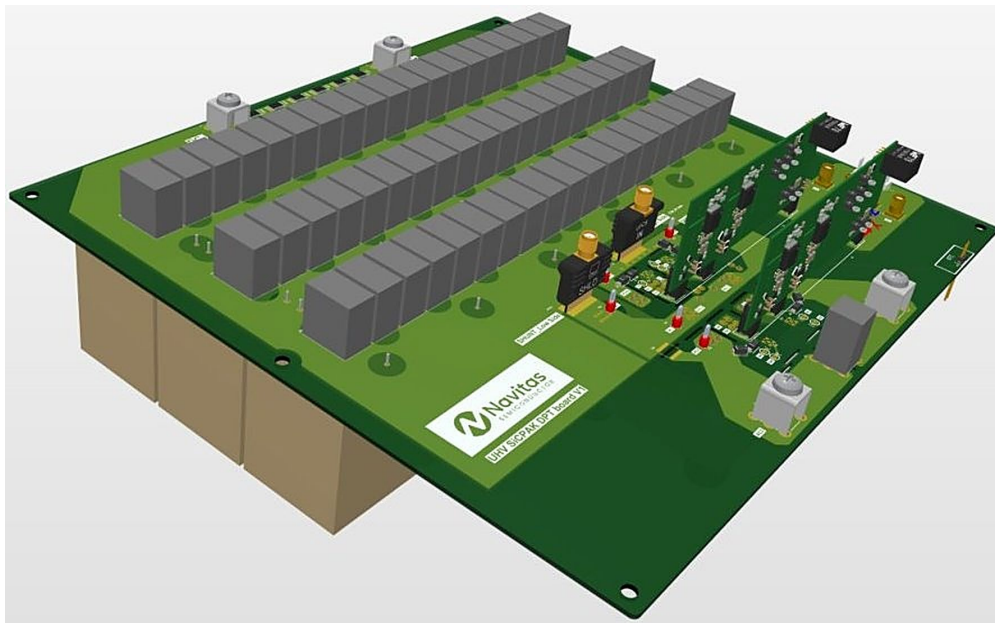


Fig. 1. UHV SiCPAK™ G+ DPT evaluation board EVB-UHVSIC-GB-E-DPT-1 (board V1), isometric view.

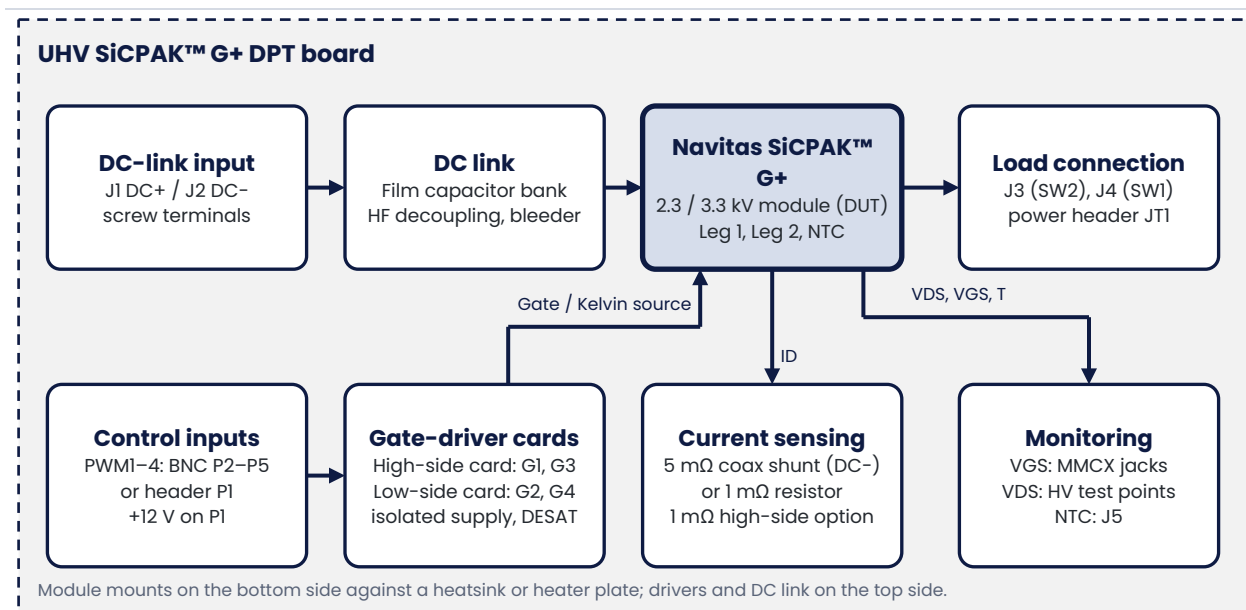


Fig. 2. Board block diagram.

The board is compatible with all Navitas UHV SiCPAK™ G+ 2.3 kV and 3.3 kV modules (Fig. 3). Table 1 lists the supported part numbers; each part is also available as a **-T** version with pre-applied thermal interface material.



Fig. 3. Navitas UHV SiCPAK™ G+ module (2.3 kV / 3.3 kV), the device under test for this board.

Table 1. Supported Navitas modules.

Module class	Navitas part number	Typical DPT bus	Technology
2.3 kV SiCPAK™ G+	G4H11MT23GB4 / -T	up to 1500 V	Gen-4 TAP SiC MOSFET
2.3 kV SiCPAK™ G+	G4H11MT23GB4HC / -T	up to 1500 V	Gen-4 TAP SiC MOSFET
2.3 kV SiCPAK™ G+	G4H08MT23GB4 / -T	up to 1500 V	Gen-4 TAP SiC MOSFET
3.3 kV SiCPAK™ G+	G4H22MT33GB4 / -T	1800 – 2200 V	Gen-4 TAP SiC MOSFET
3.3 kV SiCPAK™ G+	G4H17MT33GB4 / -T	1800 – 2200 V	Gen-4 TAP SiC MOSFET

-T = version with pre-applied thermal interface material (TIM).

3. Board Specifications

Table 2. Absolute maximum ratings ($T_A = 25\text{ }^{\circ}\text{C}$ unless otherwise stated).

Parameter	Symbol	Conditions	Value	Unit
DC-link voltage, continuous	VDC	J1 to J2, Board V1	2000	V
Switch-node peak voltage	VSW(pk)	Including turn-off overshoot	2500	V
Pulsed load current	IP	Single double-pulse burst	DUT IDM	A
Control supply voltage	VCC	P1, +12 V to GND	12	V
DUT case temperature	TC	Heater plate	175	$^{\circ}\text{C}$
Board ambient temperature	TA	Operating	0 to 25	$^{\circ}\text{C}$

Table 3. Recommended operating conditions.

Parameter	Symbol	Min.	Typ.	Max.	Unit
DC-link voltage, 2.3 kV DUT	VDC	–	1500	1500	V
DC-link voltage, 3.3 kV DUT (Rev 2)	VDC	–	1800	2200	V
Load inductance (air core)	L	50	100	500	μH
First-pulse width	t1	5	–	100	μs
Off time between pulses	t2	2	5	10	μs
Interval between bursts	tREP	1	–	–	s

Table 4. Board characteristics.

Parameter	Value
PCB	4 layers, laminated DC+ / DC- power planes
Current sense	5 m Ω coaxial shunt or 1 m Ω resistor (low side); 1 m Ω resistor (high side)
Switch-node snubber	10 nF across each switch (optional)
DC-link bleeder	300 k Ω total
Gate drive	2 $\times$ Navitas isolated plug-in gate-driver cards with DESAT
PWM inputs	4 $\times$ BNC or 2 $\times$ 6 header; +12 V control supply

4. Hardware Description

4.1 Power stage

The Navitas UHV SiCPAK™ G+ module (device under test, Table 1) contains two half-bridge legs. The leg 1 switch node (SW1) is brought out to J4 and the leg 2 switch node (SW2) to J3. One snubber

capacitor sits across each switch to damp switch-node ringing. Because the snubbers add to the measured Eon, fit or remove them consistently and record it with the data.

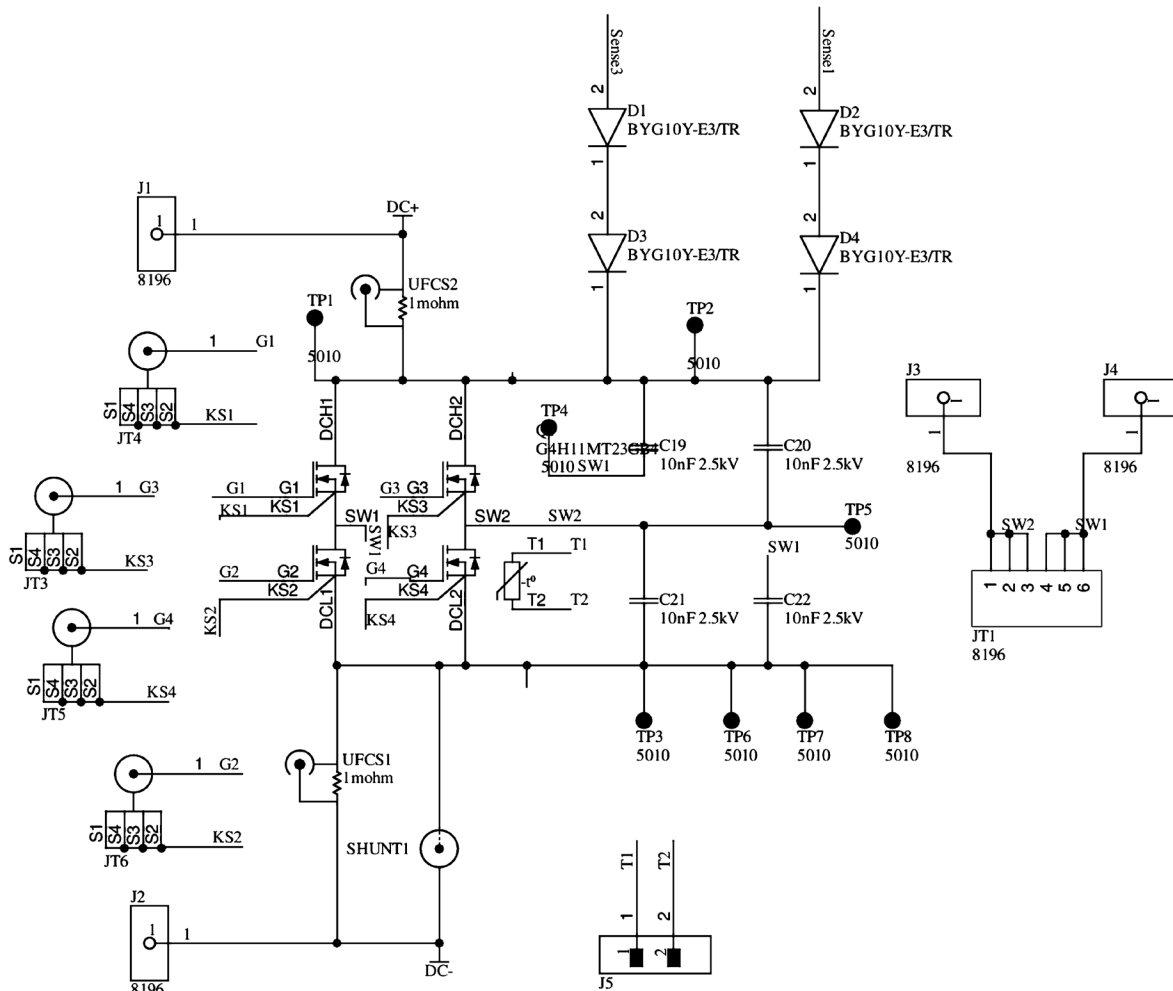


Fig. 4. Power stage, current sensing and DESAT sensing.

4.2 Current sensing

- **5 mΩ coaxial shunt (SHUNT1):** in the DC- return; preferred for high-bandwidth Eon and Eoff.
- **1 mΩ resistor (UFCS1):** alternative in the same path. Fit only one of the two.
- **1 mΩ resistor (UFCS2):** in the DC+ path for high-side DUT tests; measure with an isolated probe.

4.3 Gate drive and protection

Two Navitas plug-in gate-driver cards share a 12-pin interface: +12 V, GND, two PWM inputs, two gate / Kelvin-source pairs and two DESAT sense pairs. The high-side card (board position U1) drives G1 and G3, and the low-side card (U2) drives G2 and G4. Each card has its own isolated supplies and gate resistors, so RG or the driver can be changed without touching the power stage. DESAT sensing uses two series high-voltage diodes per switch.

Table 5. Connectors and interfaces.

Function	Designator	Description
DC-link input	J1 / J2	DC+ / DC- screw terminals
Load inductor	J3 / J4, JT1	SW2 / SW1 screw terminals; 6-pin power header
Control	P1	2×6 header: +12 V, GND, PWM1 – PWM4
PWM inputs	P2 – P5	BNC: P2 → G3, P3 → G1, P4 → G4, P5 → G2
VGS probing	JT3 – JT6	MMCX: JT3 G3, JT4 G1, JT5 G4, JT6 G2
Voltage probing	TP1 – TP8	Test points on DCH, DCL, SW1, SW2
Temperature	J5	Module NTC

4.4 UGD gate-driver card

The board uses two Navitas UGD V1.0 gate-driver cards (Fig. 5). Each card has two fully isolated channels, labelled LS and HS on the card schematic; because both channels are isolated, either one can drive a high-side or a low-side switch. Each channel combines a UCC218915-Q1 isolated gate driver with an external complementary MOSFET booster for high peak gate current, an active Miller clamp, DESAT short-circuit protection with soft turn-off and its own isolated bias supply (Table 6).

The two PWM inputs of a card are cross-coupled: each driver receives its own PWM on IN+ and the other channel's PWM on IN-, so the two outputs of one card can never be on at the same time. The on-card gate resistors set the switching speed; change them to tune dv/dt and di/dt , and record the values with the measured data.

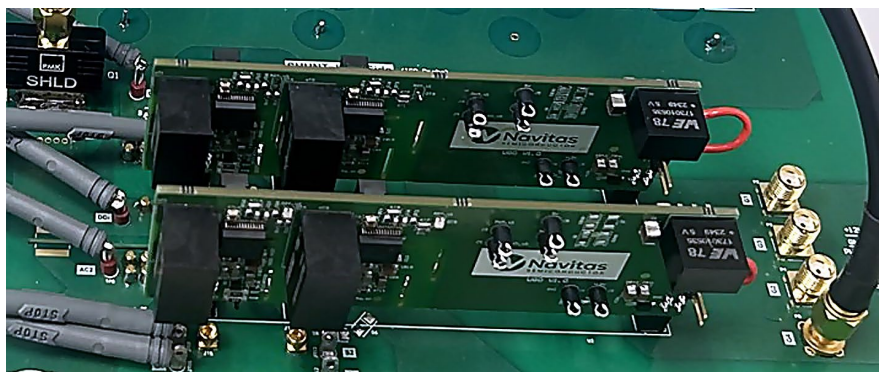


Fig. 5. The two UGD V1.0 gate-driver cards fitted on the DPT board.

Table 6. UGD gate-driver card summary.

Item	Value
Isolated gate driver	TI UCC218915-Q1, one per channel
Output booster	Nexperia BUK6D43-40P (P-channel, turn-on) and BUK6D23-40E (N-channel, turn-off)
Gate-drive voltage	+18 V / -5 V
Isolated bias supply	Murata MGJ2D121805SC, 2 W, 5.2 kV DC isolation, one per channel
Gate resistors (fitted)	RG(on) = $2 \times 3.3 \Omega$ in parallel (1.65 Ω); RG(off) = $2 \times 1 \Omega$ in parallel (0.5 Ω)
Active Miller clamp	BUK6D23-40E, driven from the driver CLMPE pin through 10 Ω
Short-circuit protection	DESAT with 100 pF blanking capacitor and two high-voltage diodes on the main board; soft turn-off through 30 Ω
Gate-source resistor	10 k Ω at each card output
Input supply	+12 V with reverse-polarity diode and common-mode chokes; on-card 5 V module for the driver input side
Status LEDs	Power (purple); RDY (green) and FLT (red) per channel
Isolation spacing	≥ 6.2 mm copper spacing primary to secondary; ≥ 6.8 mm between channels
PCB	103 mm $\times$ 36 mm, 6 layers

 Table 7. UGD connector pinout (4-pin 2 $\times$ 2 Würth 61300421021 headers).

Connector	Pin assignment
P3 (input)	1: +12 V · 2: GND · 3: PWM, HS channel · 4: PWM, LS channel
P4 (LS channel output)	1: gate · 2: Kelvin source · 3: DESAT sense · 4: Kelvin source
P5 (HS channel output)	Same as P4, for the HS channel

5. Test Setup and Connections

Fig. 6 shows the bench connections. Power and control connections are drawn solid; measurement probes are dashed. Everything at high voltage sits inside an interlocked enclosure.

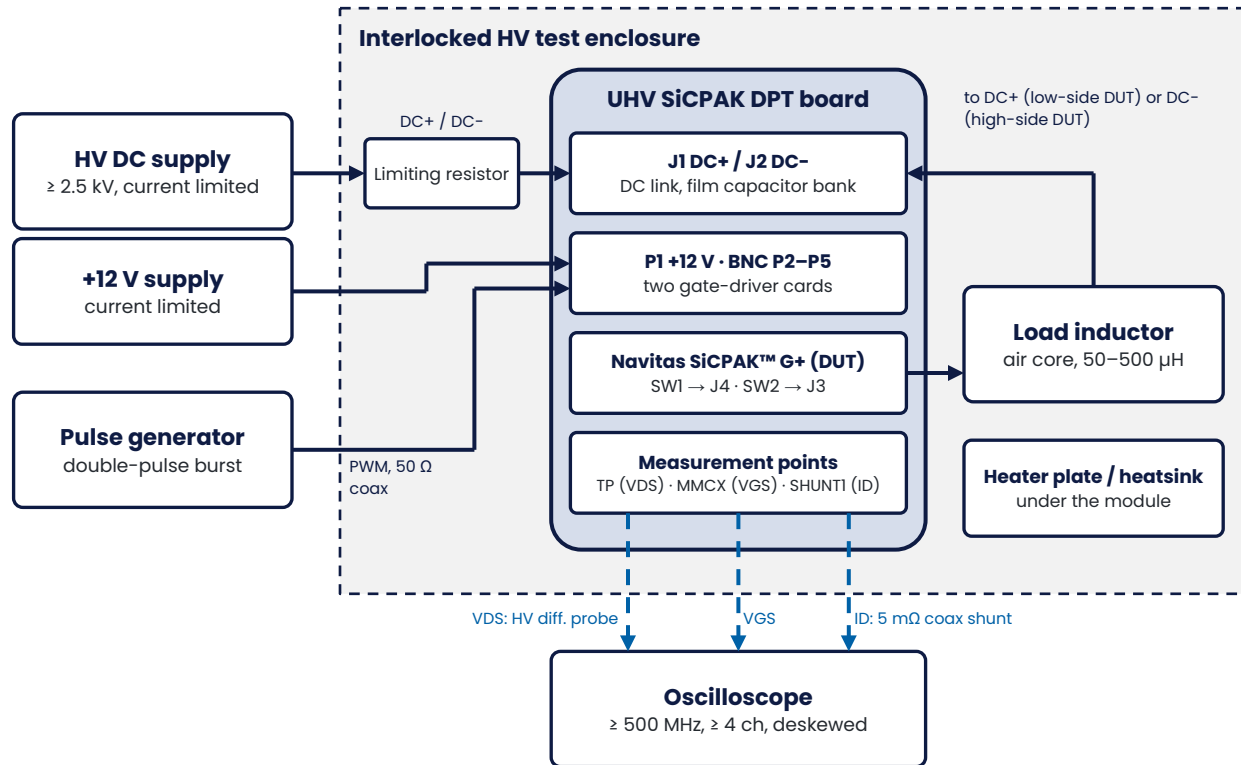


Fig. 6. Double-pulse test setup and connections.

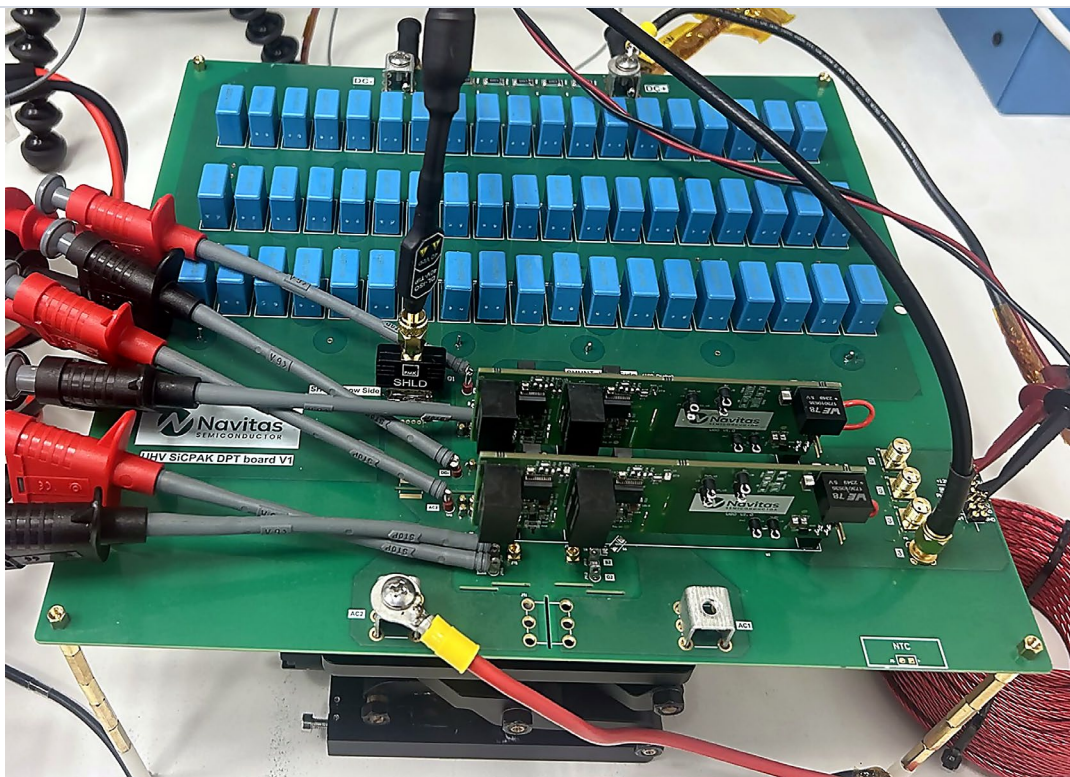


Fig. 7. EVB-UHVSIC-GB-E-DPT-1 on the test bench: gate-driver cards fitted, VGS and VDS probes connected.

Table 8. Connection list.

From	To (board)	Note
HV DC supply (+ / -)	J1 (DC+) / J2 (DC-)	Through a series limiting resistor; HV-rated cable
Load inductor, end A	J4 (SW1) or J3 (SW2)	Leg under test
Load inductor, end B	J1 (DC+) or J2 (DC-)	DC+ for a low-side DUT, DC- for a high-side DUT
+12 V supply	P1	Current-limited
Pulse generator	BNC P2 – P5	50 Ω coax, one channel per switch
Scope – VDS	Test points across DUT	HV differential probe, ≥ 6 kV
Scope – VGS	MMCX JT3 – JT6	Optically isolated probe for high side
Scope – ID	SHUNT1	5 m Ω coaxial shunt output
Heater plate	Module baseplate	Read case temperature on J5 (NTC)

Table 9. DUT selection.

DUT	Inductor	Pulsed PWM	Held-off gate	VGS probe
Leg 1 low side (G2)	J4 $\rightarrow$ DC+	P5 (PWM4)	G1	JT6

DUT	Inductor	Pulsed PWM	Held-off gate	VGS probe
Leg 1 high side (G1)	J4 → DC-	P3 (PWM2)	G2	JT4
Leg 2 low side (G4)	J3 → DC+	P4 (PWM3)	G3	JT5
Leg 2 high side (G3)	J3 → DC-	P2 (PWM1)	G4	JT3

Table 10. Recommended equipment.

Equipment	Recommended specification
HV DC power supply	≥ 2.5 kV, adjustable current limit
Load inductor	50 – 500 μ H air core, ≥ 4 kV insulation
Pulse generator	2 – 4 channels, burst mode
Oscilloscope	≥ 4 channels, ≥ 500 MHz, 12-bit preferred
Probes	HV differential (≥ 6 kV), optically isolated VGS, 5 m Ω coaxial shunt
Heater plate	Up to 175 °C with controller
Discharge stick and meter	Rated ≥ 5 kV

6. Operating Procedure

6.1 Preparation (power off)

1. Press-fit the SiCPAK™ G+ module into its footprint on the bottom side and mount the heatsink or heater plate with thermal interface material.
2. Fit one current-sense option and decide whether the snubbers are fitted; record both.
3. Plug in the high-side and low-side gate-driver cards and set the gate resistors.
4. Make all connections in Fig. 6 with the HV supply output off.
5. Close the enclosure and check the interlock.

6.2 Low-voltage check

1. Apply +12 V to P1 and check the supply current.
2. Without HV, send one pulse and check the VGS swing on the DUT gate.
3. Check that the opposite gate stays at negative bias.

6.3 Double-pulse test

The first pulse builds current in the load inductor and the DUT turns off at the test current (E_{off}). The current then freewheels through the opposite body diode, and the second pulse turns the DUT on again at the same current (E_{on} , E_{err}).

1. Program a two-pulse burst, single shot, with a 2 – 10 μ s off time.

2. Raise VDC in steps (for example 100 V, 500 V, then target) and fire once per step.
3. At target VDC, lengthen the first pulse until the scope shows each test current.
4. Save waveforms for every point and wait at least 1 s between bursts.
5. For temperature sweeps, set the heater plate and wait for a stable NTC reading.

6.4 Shutdown

1. Turn off the HV supply output and wait for the bleeder to discharge the DC link.
2. Open the enclosure only below 60 V and short DC+ to DC- with the discharge stick.
3. Remove +12 V last.

7. Measurement and Data Analysis

Switching energies are calculated by the oscilloscope from the deskewed VDS and ID waveforms over the windows in Table 11, following Navitas datasheet conventions.

Table 11. Switching-energy integration windows.

Quantity	Start	End
Eoff	VGS falls to 90 % of VGS(on)	ID falls to 2 % of Itest
Eon	VGS rises to 10 % of VGS(on)	VDS falls to 2 % of VDC
Err	Diode current crosses zero	Reverse current returns to 2 % of IRRM

- **Report:** Eon, Eoff and Err against ID and against RG, at TC = 25 °C and 150 – 175 °C.
- **Record:** VDC, gate voltages, RG, inductance, snubber status and shunt type with every dataset.
- **Timing:** td(on), tr, td(off), tf, dv/dt, di/dt and peak VDS overshoot from the same waveforms.

8. Layout Guidelines

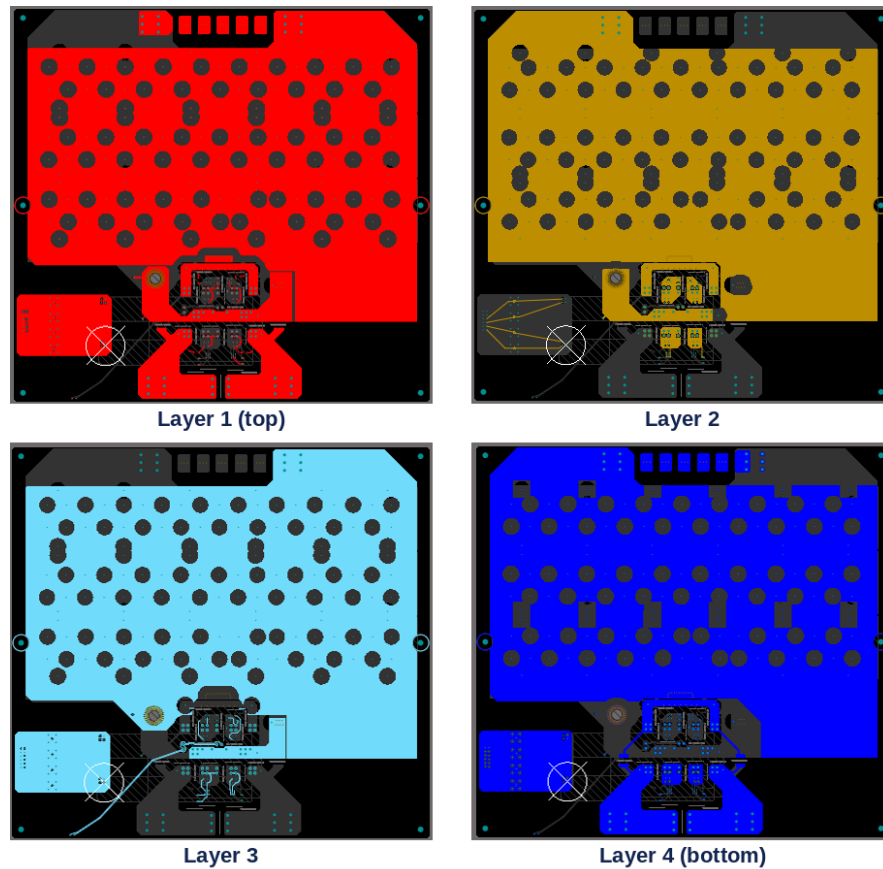


Fig. 8. PCB copper layers L1 to L4.

9. Safety

WARNING – high voltage: the board operates at up to 2000 V DC and its DC link stores enough energy to cause death or serious injury. Operate only inside a closed, interlocked enclosure, by trained personnel. Confirm the DC link is below 60 V before touching the board, use a current-limited supply with a series resistor, wear eye protection and beware of hot surfaces above 150 °C.

10. Engineering Bill of Materials

Table 12. Navitas parts.

Item	Designator	Qty	Description	Navitas part number
1	Q1	1	2.3 kV SiCPAK™ G+ half-bridge module	G4H11MT23GB4
2	Q1 (alt.)	1	3.3 kV SiCPAK™ G+ half-bridge module	G4H22MT33GB4

Passive components and connectors are standard parts; the full manufacturing BOM is available from Navitas on request.

11. Conclusion

The UHV SiCPAK™ G+ DPT evaluation board (EVB-UHVSIC-GB-E-DPT-1) gives one fixture for characterizing Navitas 2.3 kV and 3.3 kV SiC modules. Its laminated low-inductance loop, flexible DUT selection, plug-in gate drivers and precise measurement points produce clean, repeatable switching data for datasheets, gate-driver optimization and converter design.

Revision History

Revision	Date	Description
0.1	October 2026	Preliminary release.

Additional Information

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Contact: info@navitassemi.com